

# Compal Confidential

## NIMUA/UB

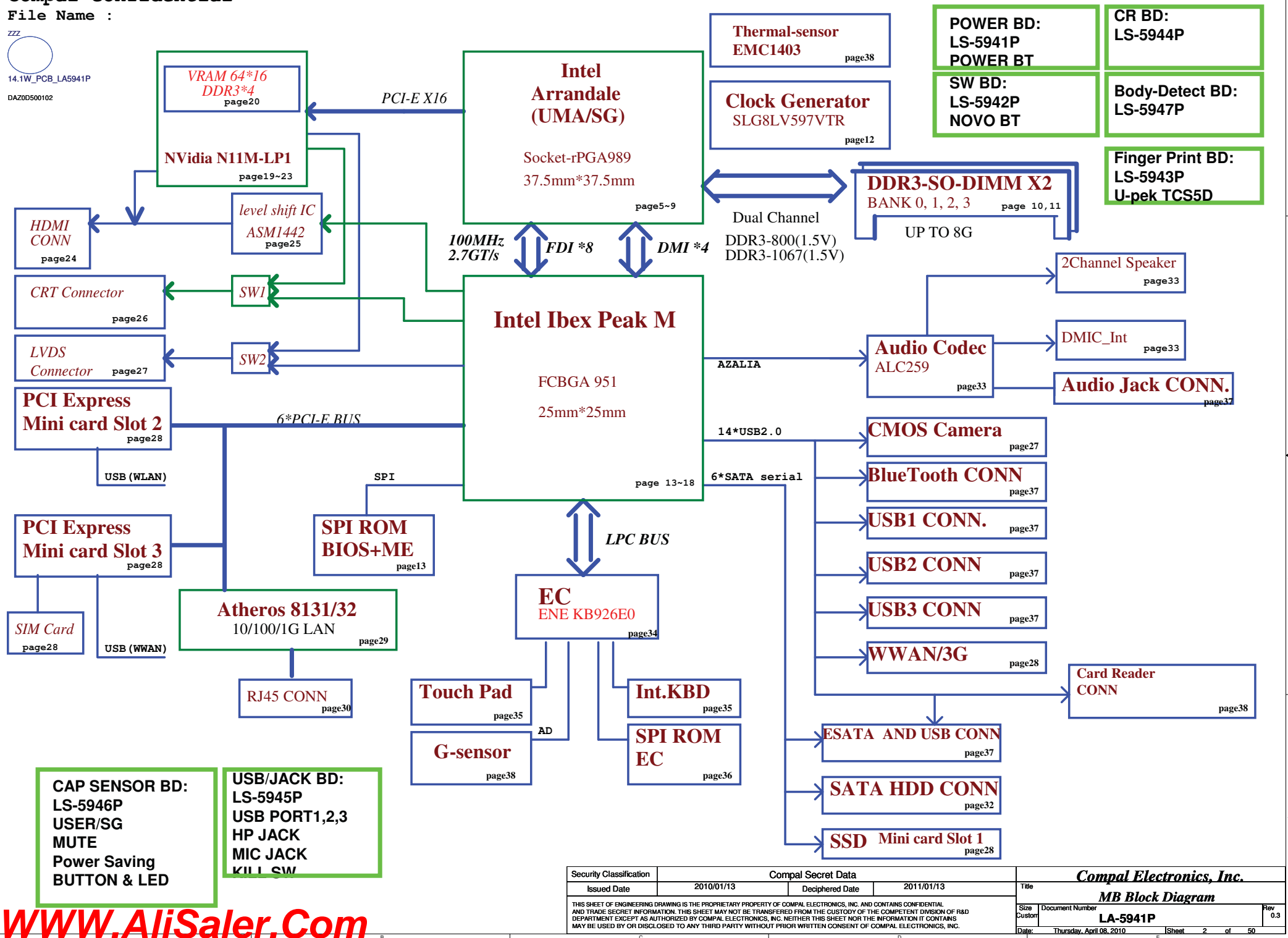
### Schematics Document

### Arrandale

with Intel IBEX PEAK-M core logic

REV : 0 . 3

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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title Cover Sheet		
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DDR3 Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+0.75VS
				+1.05VS
				For SG
				+3VS_DELAY
				+1.8VS_VGA
				+1.5VS_VGA
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	RAM M2	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	N11x Thermal Sensor	EMC1403	Cap sensor board	ALS	PCH
SMB_EC_CK1	KB926	✗	V	✗	✗	✗	✗	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	✗	✗	V	✗	✗	✗	V	V	✗	V	V
SMB_EC_DA2	+3VALW		+3VALW					+3VS	+3VS		+3VS	+3VALW
SMBCLK	PCH	V	✗	✗	V	V	✗	✗	✗	✗	✗	✗
SMBDATA	+3VALW	+3VALW			+3VS	+3VS						
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW											
SML1CLK	PCH	✗	✗	V	✗	✗	✗	✗	✗	✗	✗	✗
SML1DATA	+3VALW											

PCH, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

EC, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
PCH	96/98,R/W	1001011X 1001100X
EMC1403 Thermal sensor	9A	1001101X
N-vidia Thermal sensor	9E	1001111X
ALS	70/72,R/W	0111000X 0111001X

@ FUNCTION

PVT	NON-USE
45@	(45 BOM)
100@	10/100 LAN
GIGA@	GIGA LAN
UMA HDMI@	FOR UMA HDMI components
HDMI@	FOR HDMI components
3G@	3G(WWAN) function
X76@	(X76 BOM)
ESATA@	ESATA function
CMOS@	Camera function
SSD@	SSD w/ miniPCIE socket
10M@	FOR 10M CHIP
11M@	FOR 11M CHIP
UMA@	UMA only (Arranddale)
DIS@	DIS only (Arranddale)
VGA@	FOR NVIDIA PART
HYBRID@	FOR SWITCHABLE
HU@	SWITCHABLE or UMA only
HD@	SWITCHABLE or DIS only

PCIe PORT LIST

PORT	DEVICE
1	<del>NEW CARD</del>
2	WLAN
3	LAN
4	3G
5	
6	
7	
8	

SATA PORT LIST

PORT	DEVICE
0	HDD
1	SSD
2,3	HM55 disabled
4	E-SATA
5	

USB PORT LIST

PORT	DEVICE
0	USB 1
1	USB/ESATA
2	CMOS
3	USB 2
4	
5	CARD READER
6	✗ HM55 disabled
7	✗ HM55 disabled
8	WIRELESS
9	USB 3
10	FingerPrinter
11	BT
12	
13	3G

SKU

Arrandale(dGPU)	DIS@ / 100@ for EVT
Arrandale(iGPU)	UMA@ / 100@ for EVT
Arrandale(iGPU+dGPU)	HYBRID@
SWITCHABLE	

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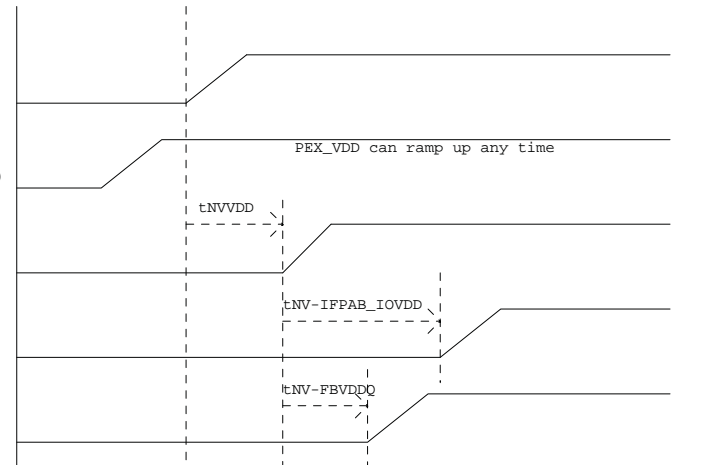
## VGA and DDR3 Voltage Rails (N11M GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	HDMI_DETECT_VGA
GPIO2	OUT	H	NV_INVTPWM
GPIO3	OUT	H	VGA_ENVDD_R
GPIO4	OUT	H	VGA_ENABLT
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	
GPIO8	I/O	L	
GPIO9	OUT	L	
GPIO10	OUT		
GPIO11	I/O	L	
GPIO12	IN	-	
GPIO13	OUT	-	
GPIO14	OUT	-	
GPIO15	IN	-	
GPIO16	OUT	-	
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	
GPIO20	IN	-	
GPIO21	IN	-	
GPIO22	IN	-	
GPIO23	I/O		

### Power Sequence

The ramp time for any rail must be more than 40us

(+3VS) VDD33  
(1.05VS) PEX\_VDD  
(+VGA\_CORE) NVVDD  
(1.8VS) IFPAB\_IOVDD  
(1.5VS) FBVDDQ

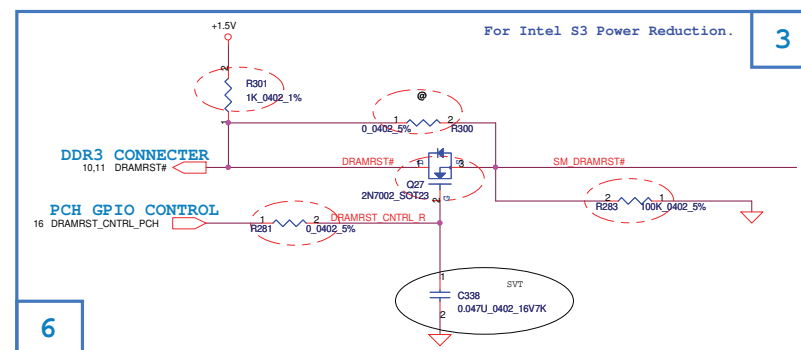
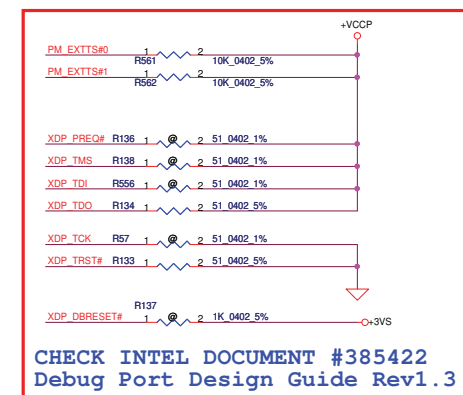
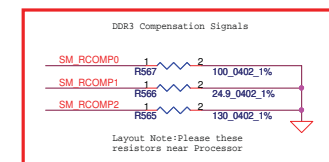
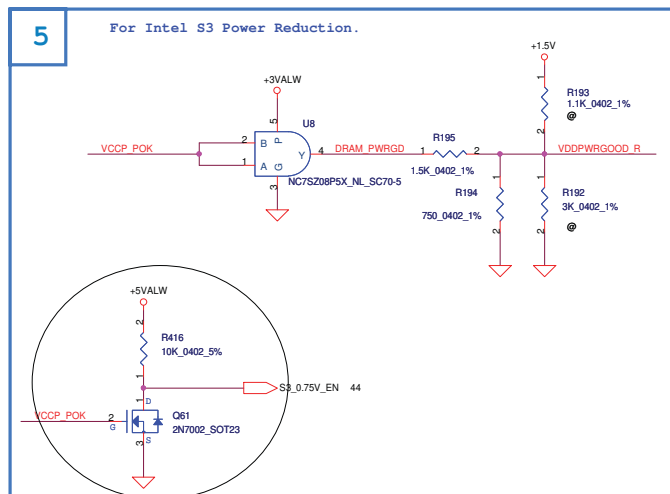
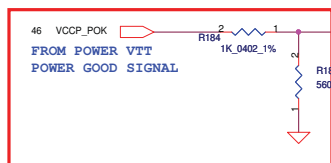
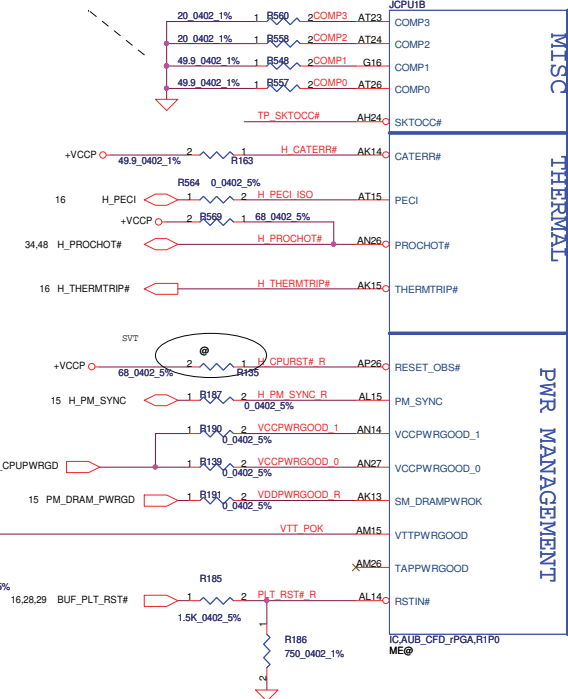


### GPIO5 GPIO6

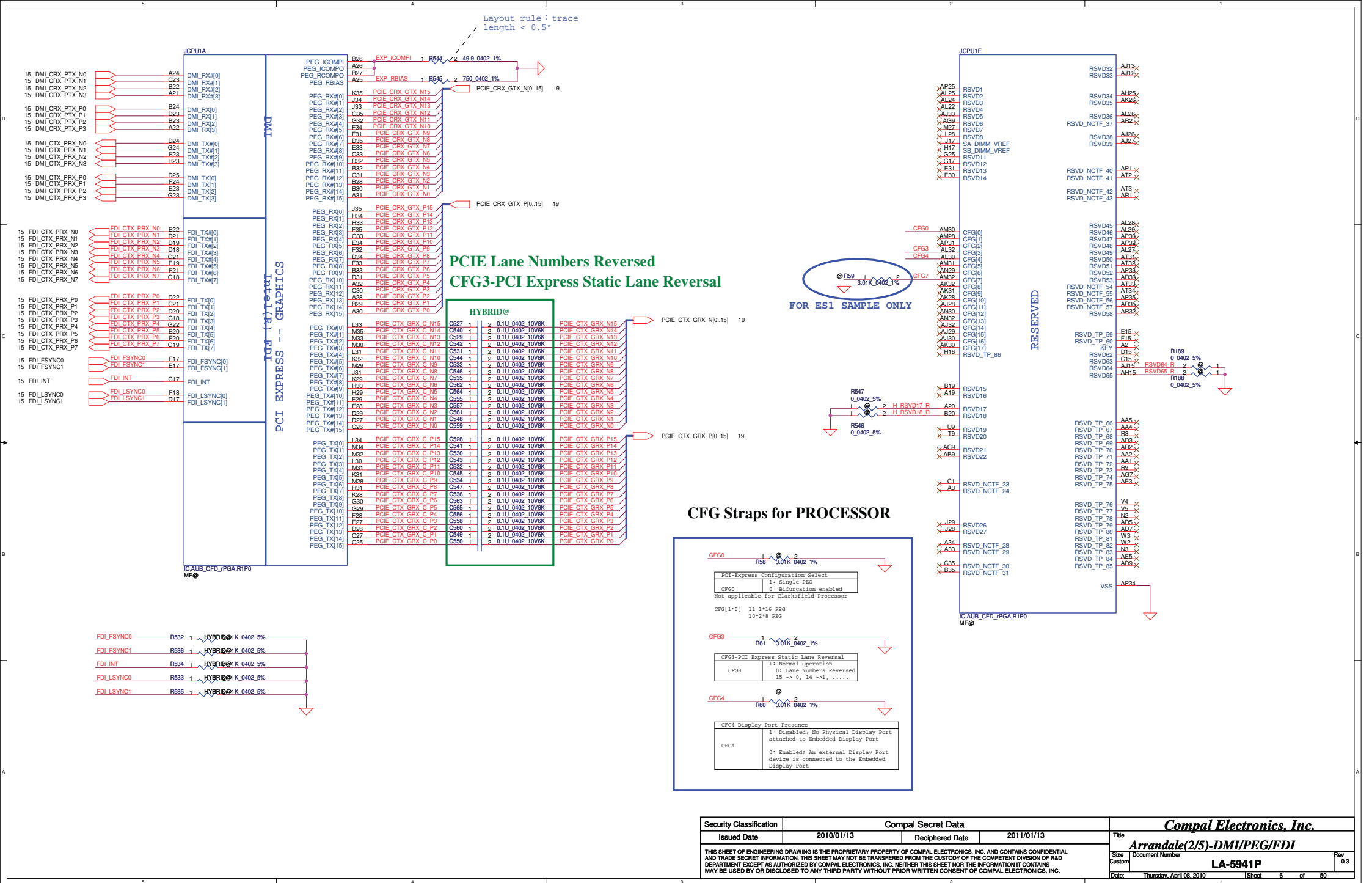
	Device ID
N11M-LP1 (40nm)	0x0A6E

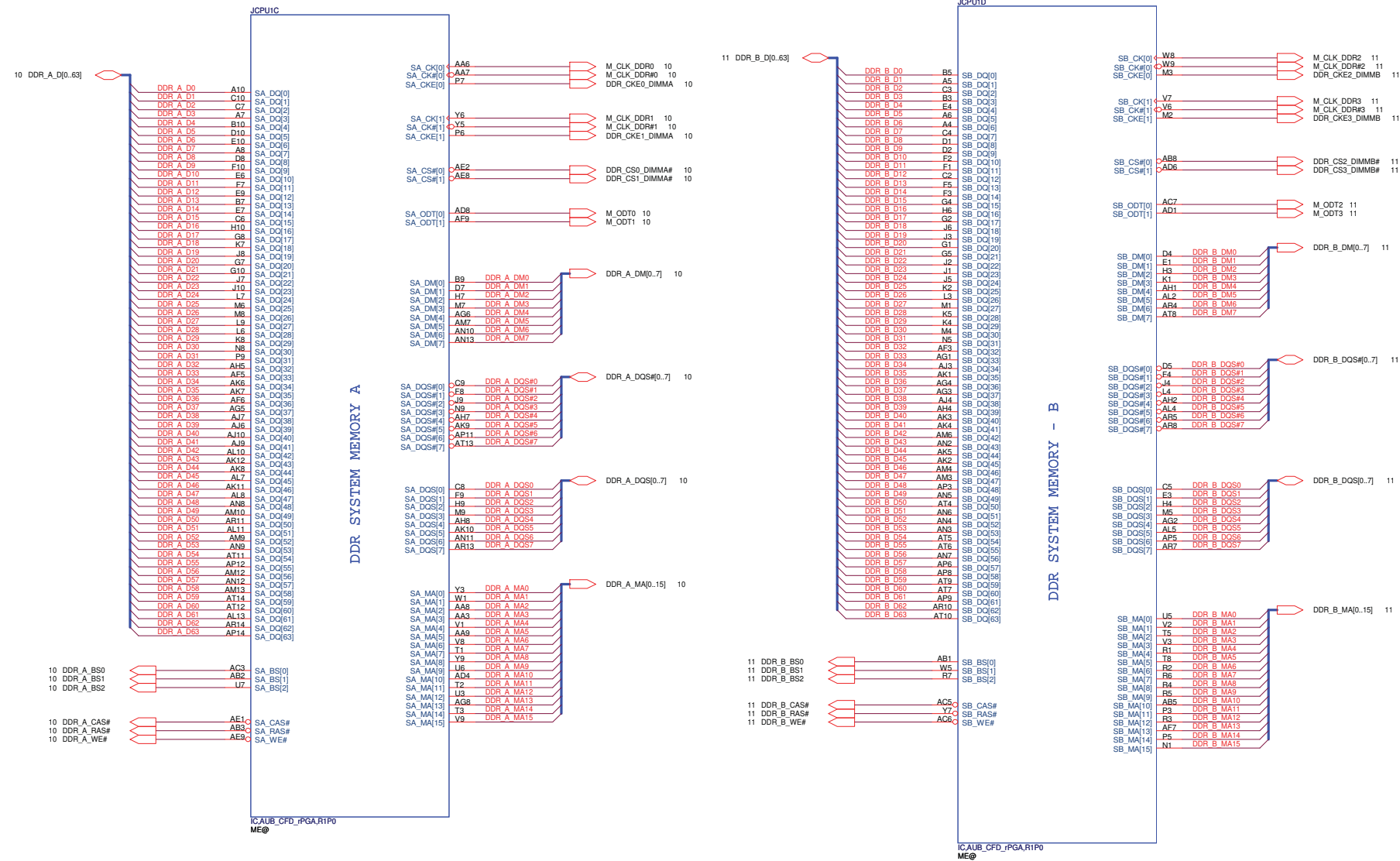
GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.86V	P0

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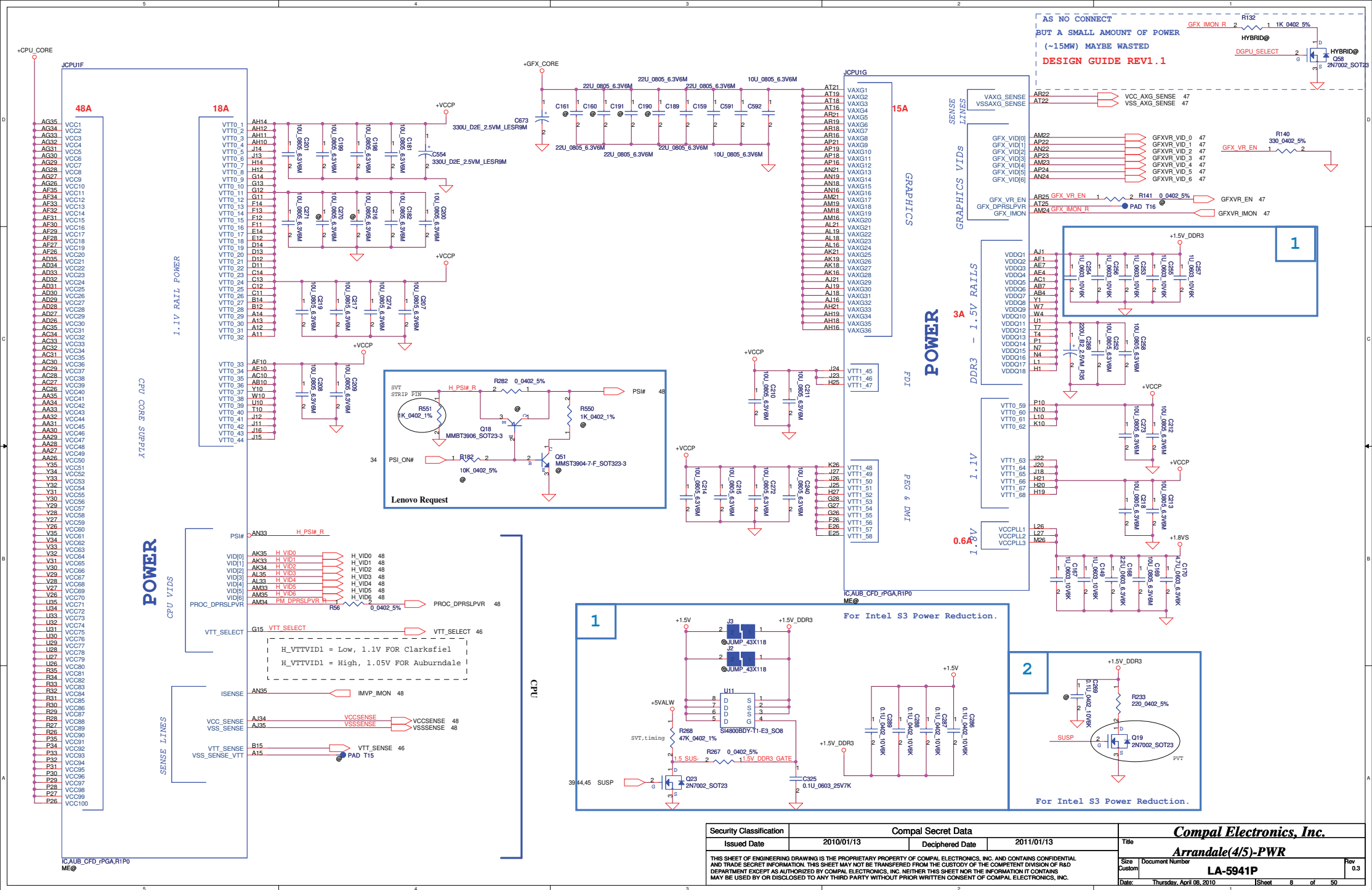
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title		Rev
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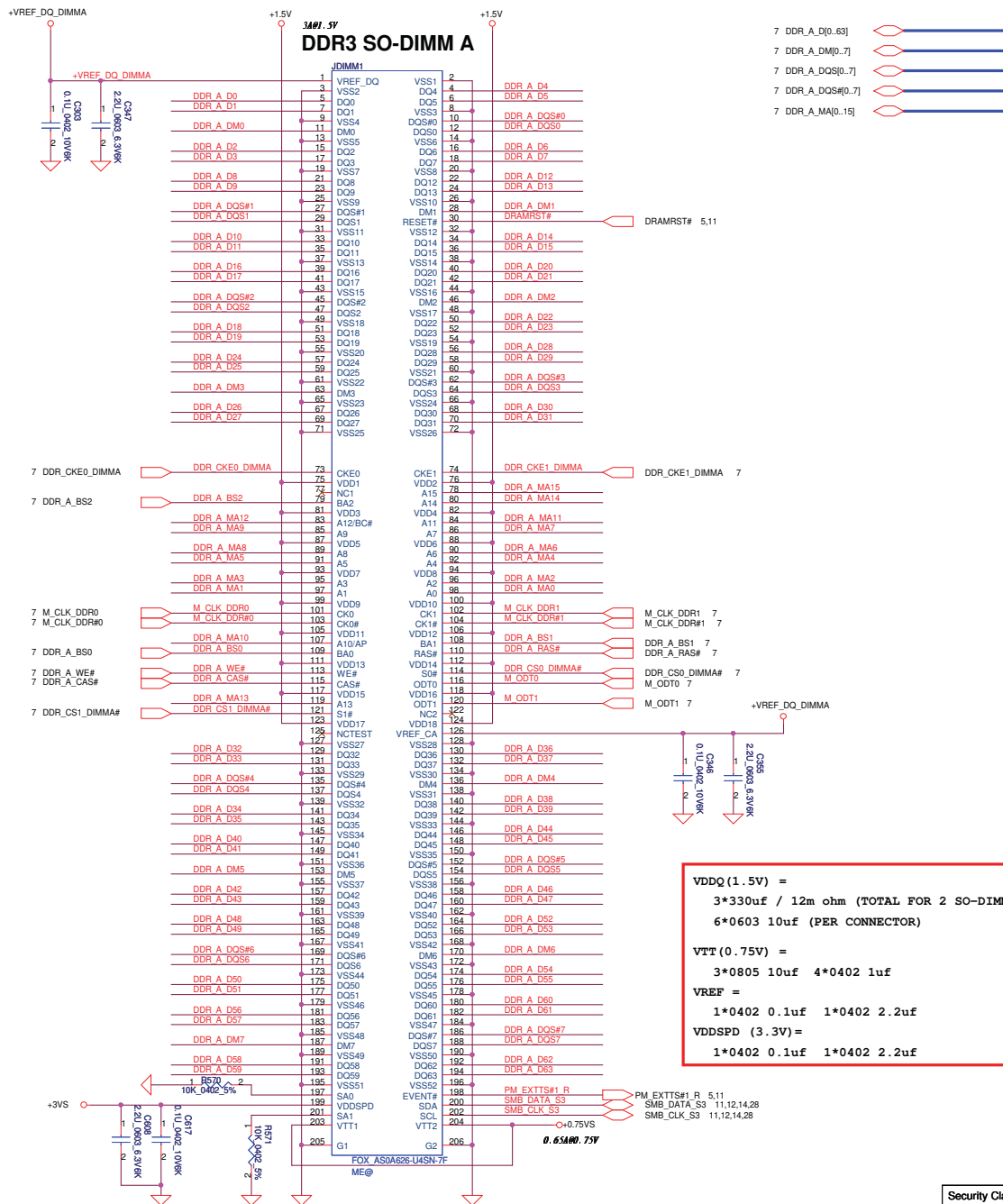
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For Arranale only +VREF\_DQ\_DIMMA supply from a external 1.5V voltage divide circuit.

07/17/2009

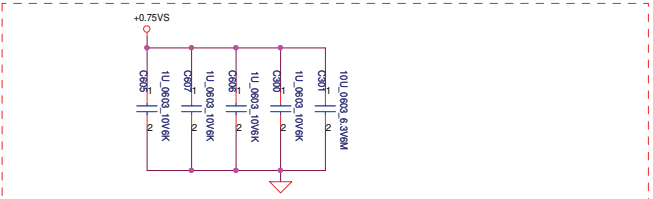
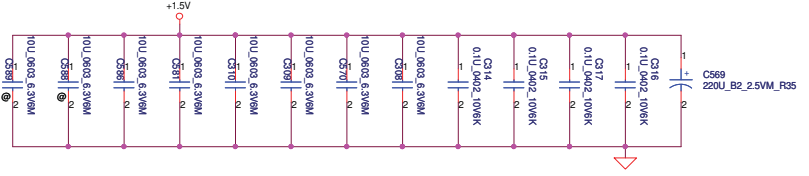
Layout Note:  
Place near DIMM

VDDQ(1.5V) =  
3\*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)  
6\*0603 10uf (PER CONNECTOR)

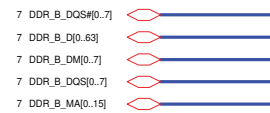
VTT(0.75V) =  
3\*0805 10uf 4\*0402 1uf

VREF =  
1\*0402 0.1uf 1\*0402 2.2uf

VDDSPD (3.3V) =  
1\*0402 0.1uf 1\*0402 2.2uf



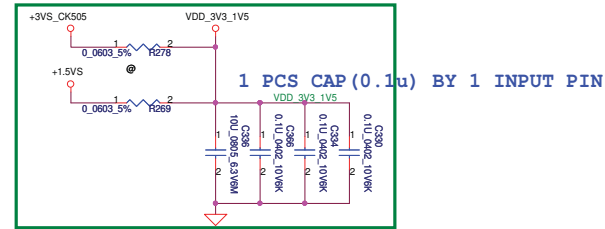
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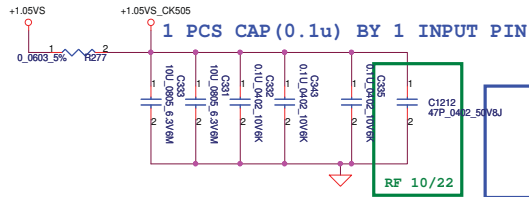
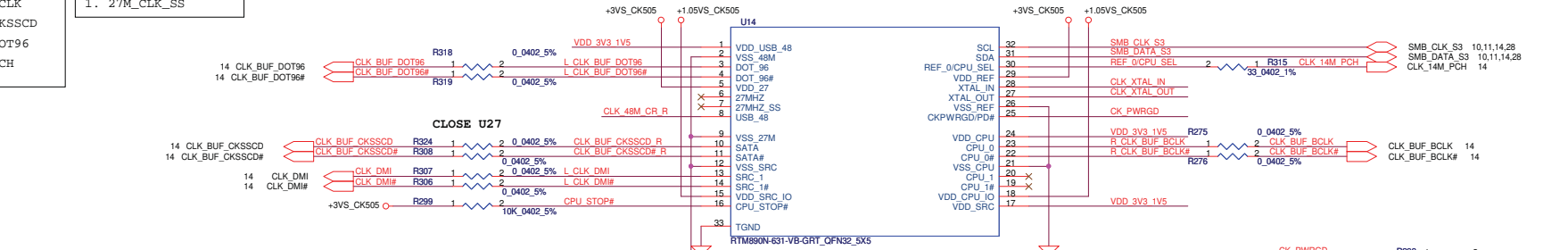
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Reserve for Low Power CLK GEN.  
RTM890N-632  
SLG8LV597VTR



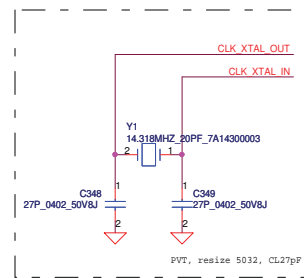
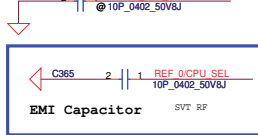
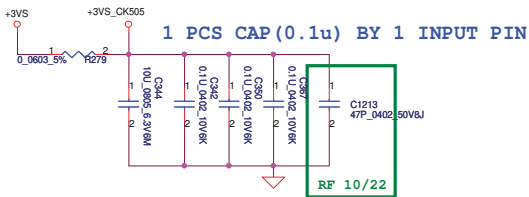
**CLK GEN TO PCH**  
1. CLK\_DMI  
2. CLK\_BUF\_BCLK  
3. CLK\_BUF\_CKSSCD  
4. CLK\_BUF\_DOT96  
5. CLK\_14M\_PCH

**CLK GEN TO VGA**  
1. 27M\_CLK  
1. 27M\_CLK\_SS

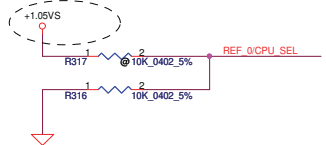


SA00003HQ10 S IC RTM890N-631-VB-GRT QFN 32P CLK GEN  
(SA00003HR00)S IC ICS9LV53199AKLFT MLF 32P CLK GEN  
S-IC SLG8SP587VTR QFN 32P CLK GEN (SA00002XY00)

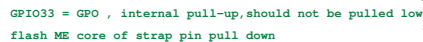
PIN8 IS GND FOR ICS3197  
PIN8 IS 48MHz FOR ICS3199



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

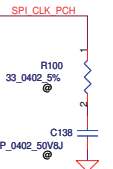
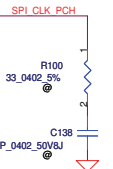


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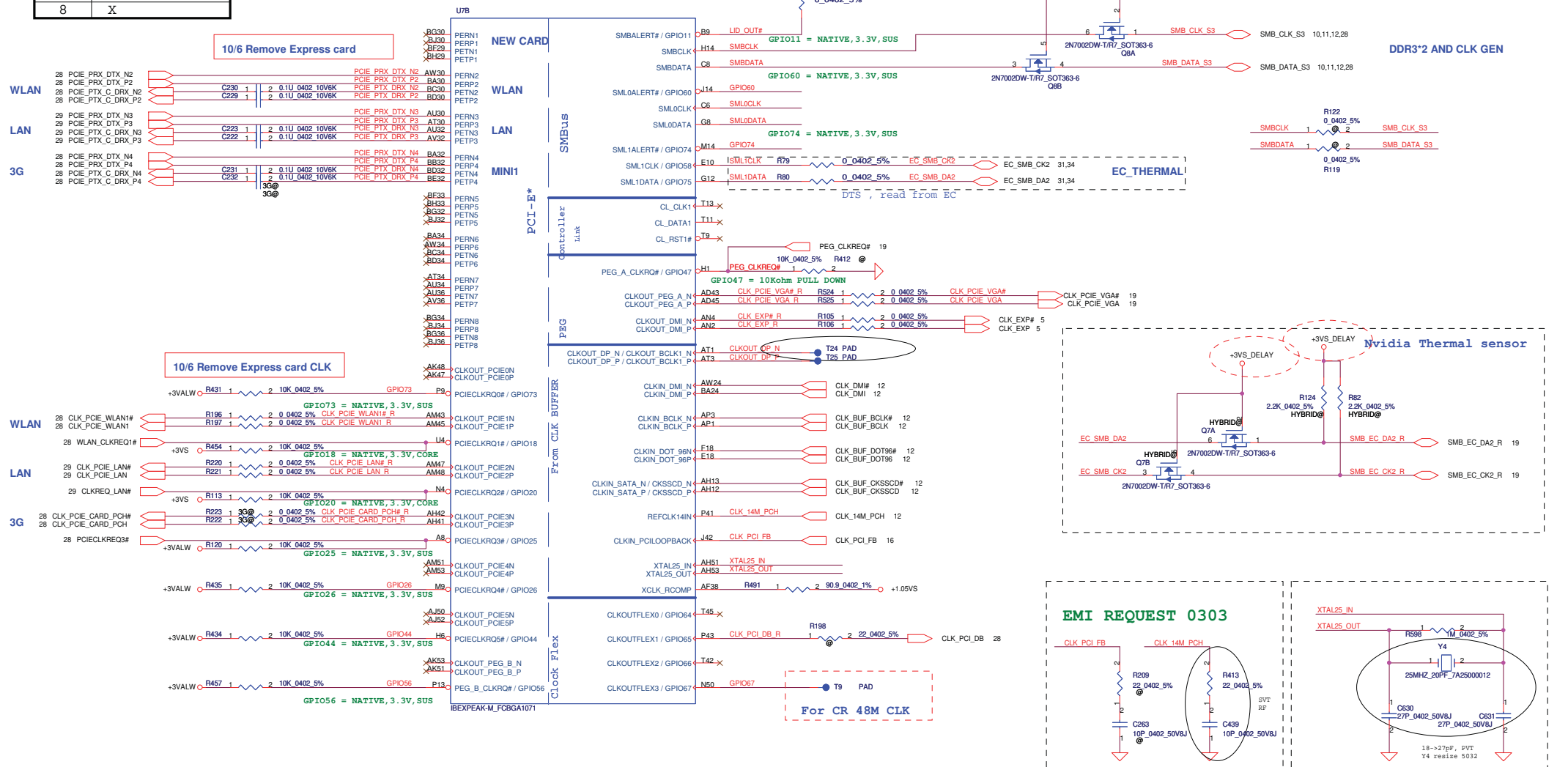
PCH JTAG TCK R114 1 2 51 0402 5% (2009, 05, 04)

FOR INTEL DPDG REV1.6 (MAY 2009)



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PCIE PORT LIST	
PORT	DEVICE
1	<del>NEW CARD</del>
2	WLAN
3	LAN
4	3G
5	X
6	X
7	X
8	X



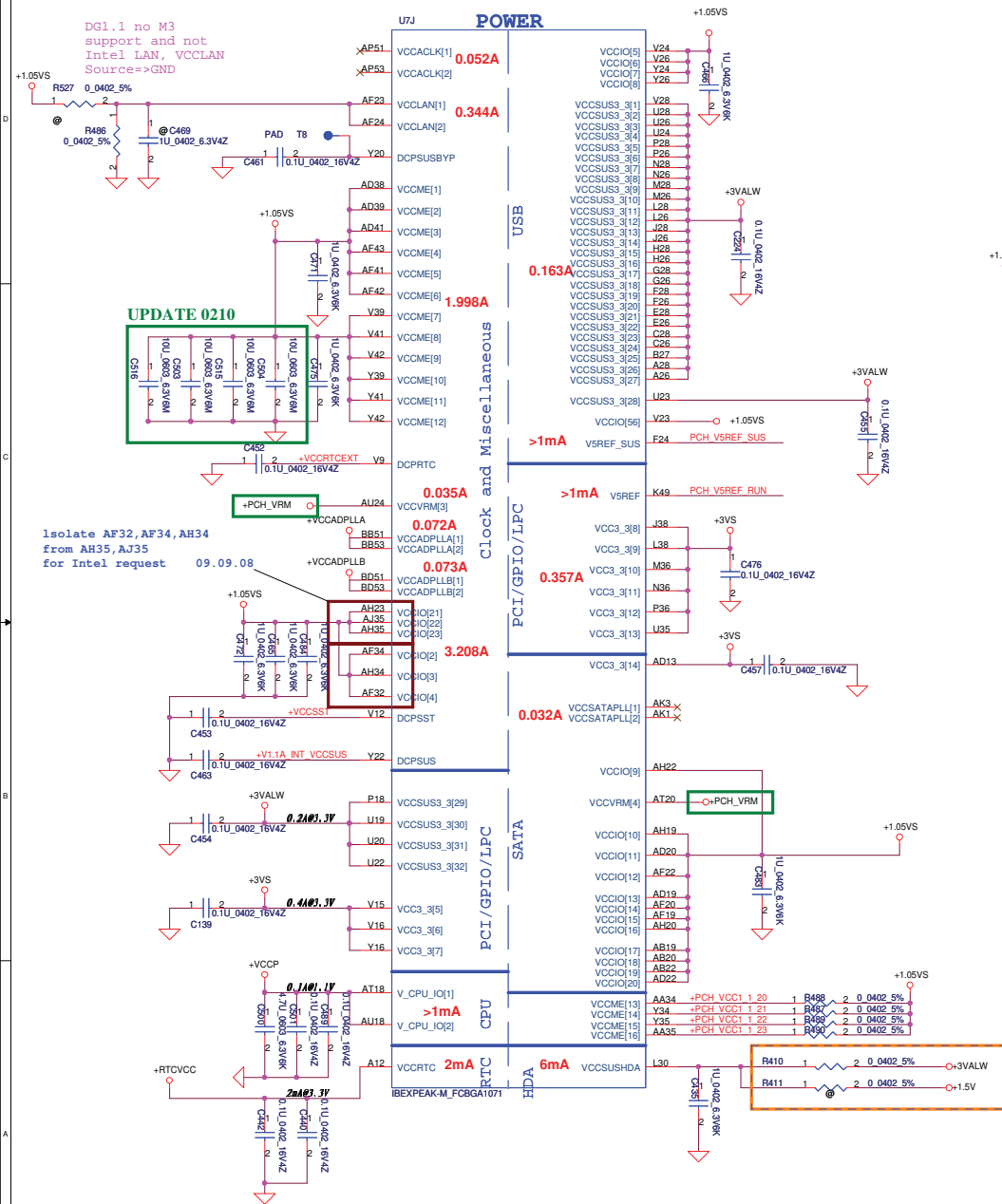
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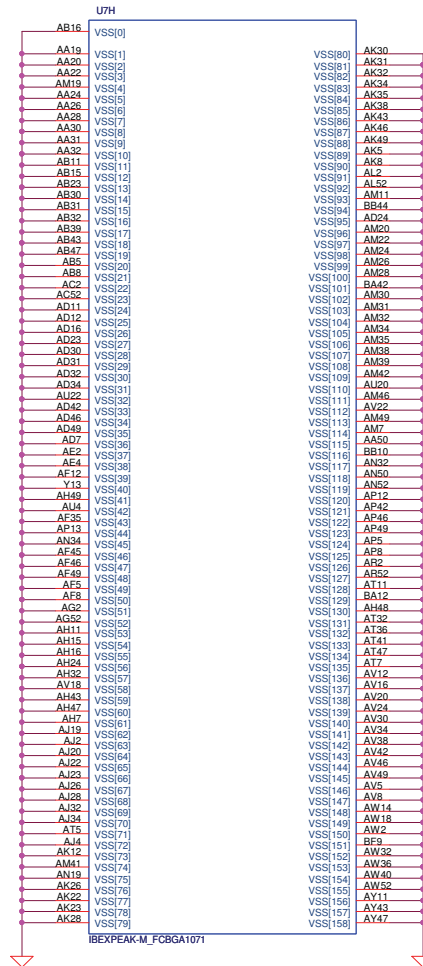
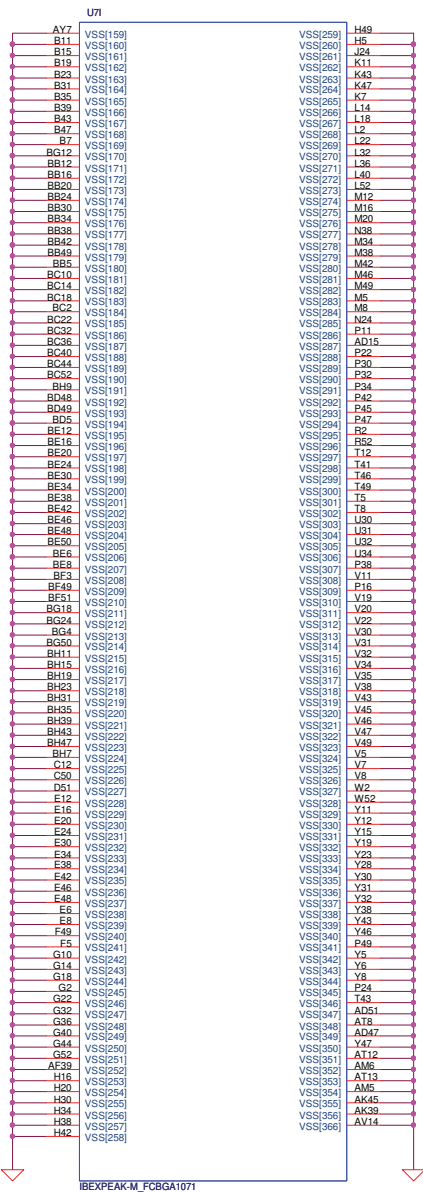








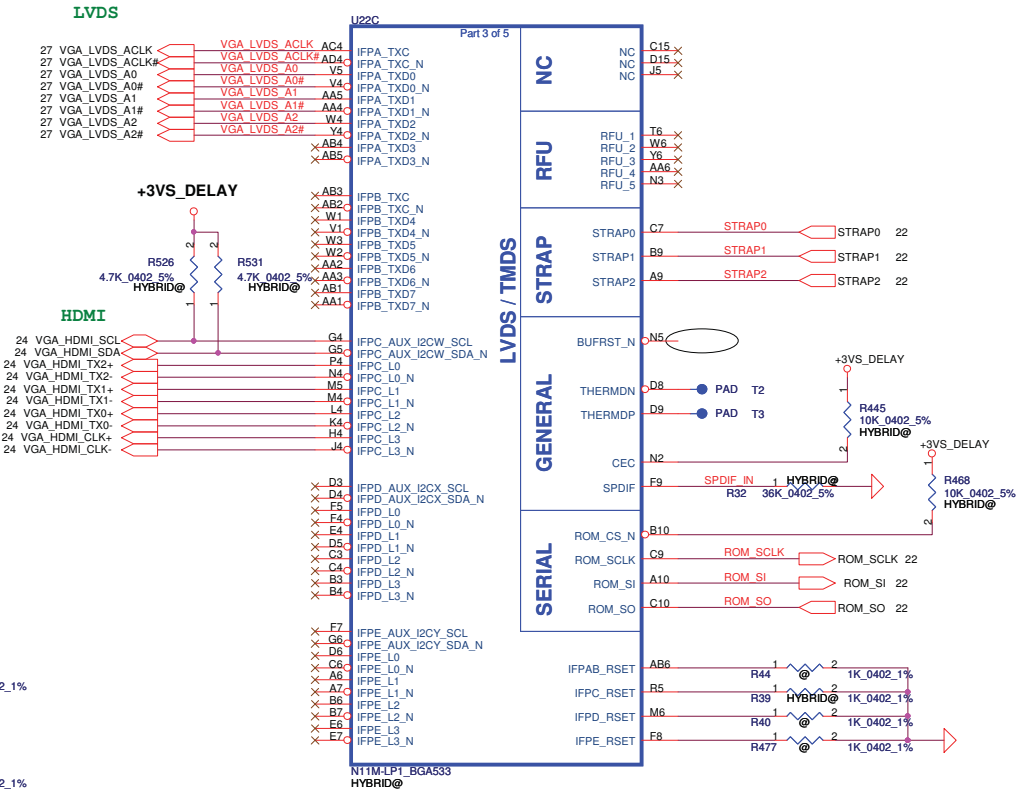
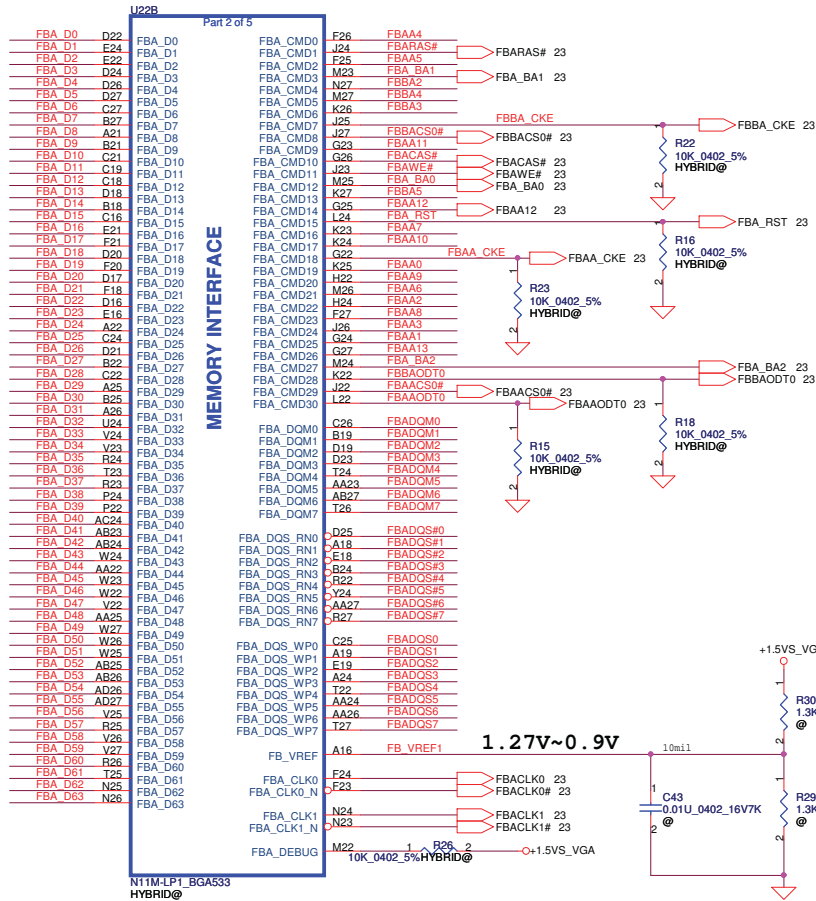
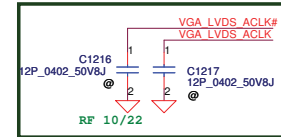




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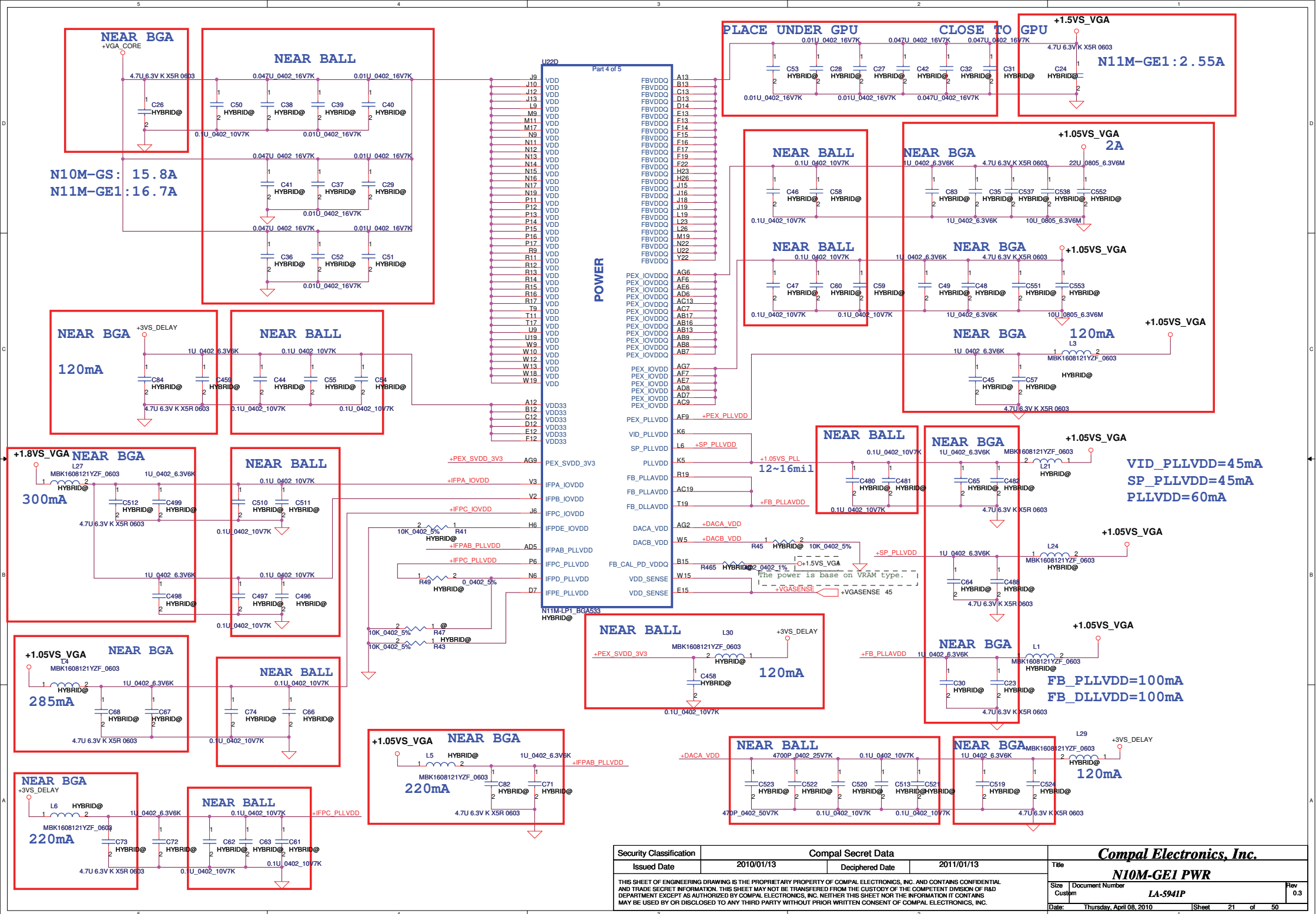


23 FBAA[0..13] FBAA[0..13]  
 23 FBBA[2..5] FBBA[2..5]  
 23 FBADQM[0..7] FBADQM[0..7]  
 23 FBADQS[0..7] FBADQS[0..7]  
 23 FBADQS# [0..7] FBADQS# [0..7]  
 23 FBAD[0..63] FBA\_DIO[63]



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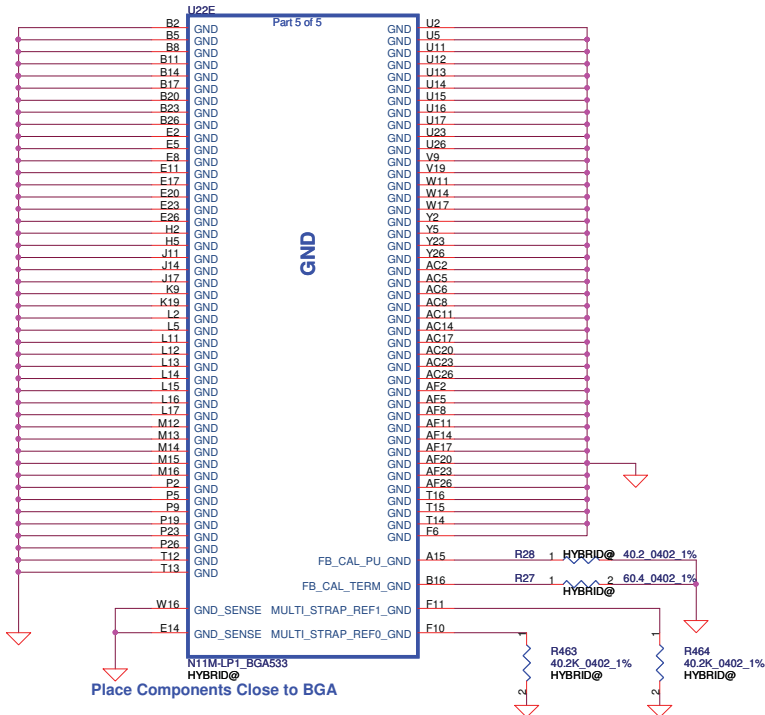
A total of 8 signals are required for GB1 strapping this includes

2 reference signals

6 physical strapping pins

4 logical strapping bits

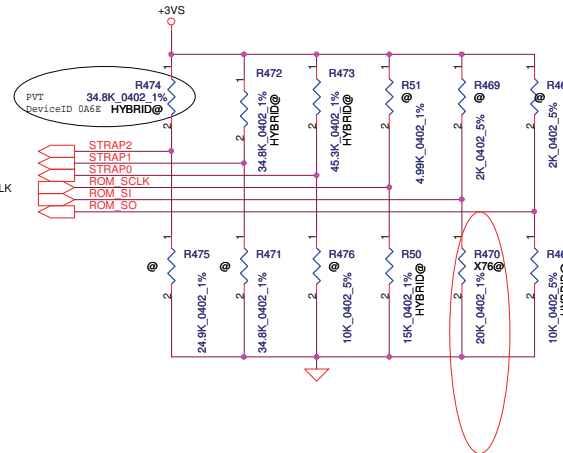
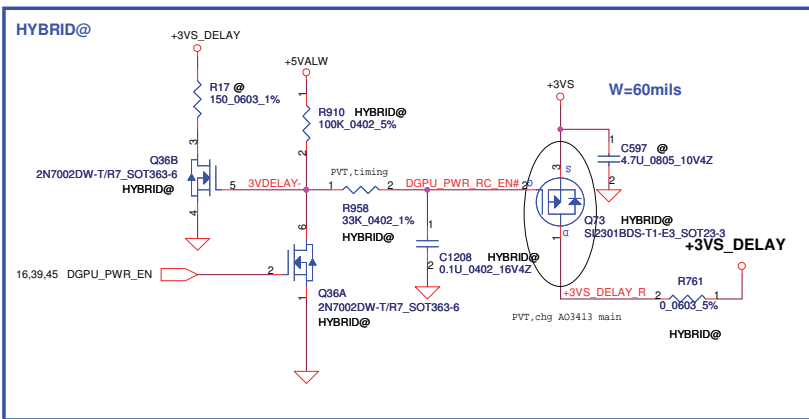
A total of 24 logical strapping bits are available



N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

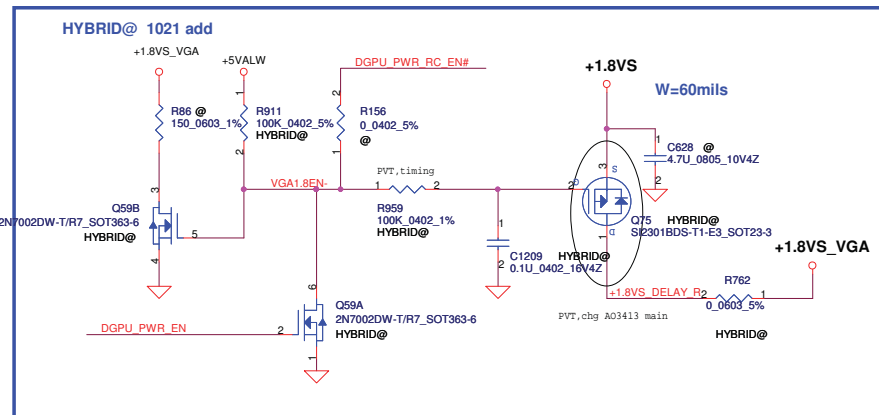
Must be used 1% resistor for driver calibration

DG-04642-001-V01(May 22, 2009)



STRAP1 use for 3GIO\_PADCFG to set 35K pull up.  
(PUN-04335-001\_V10 HW9 update)

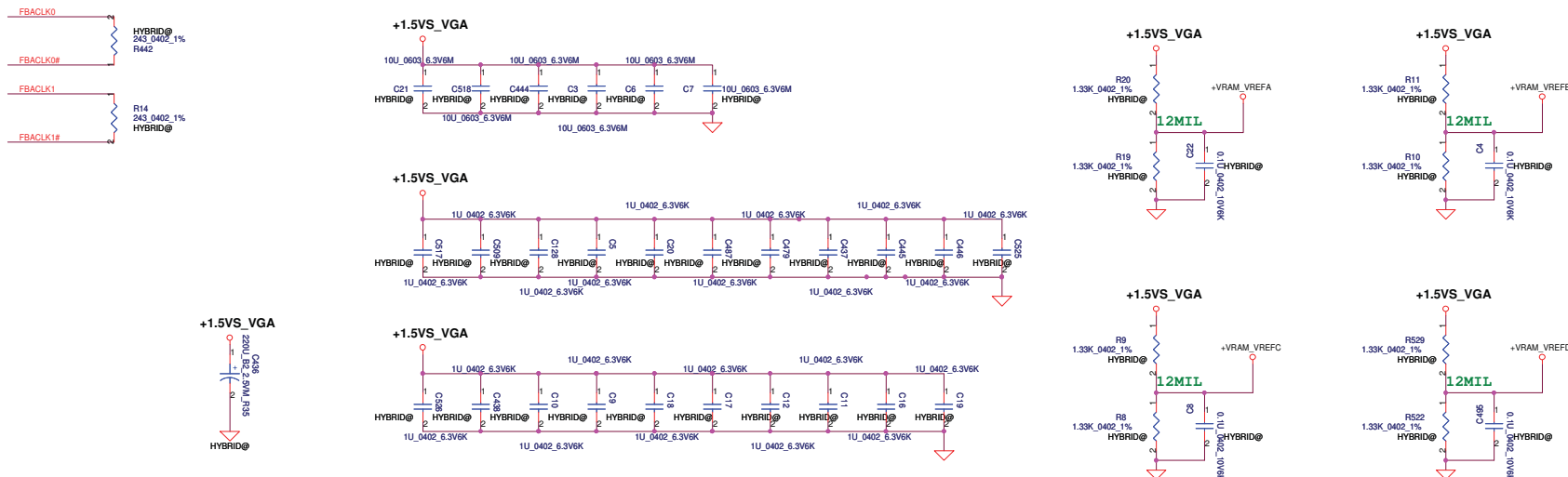
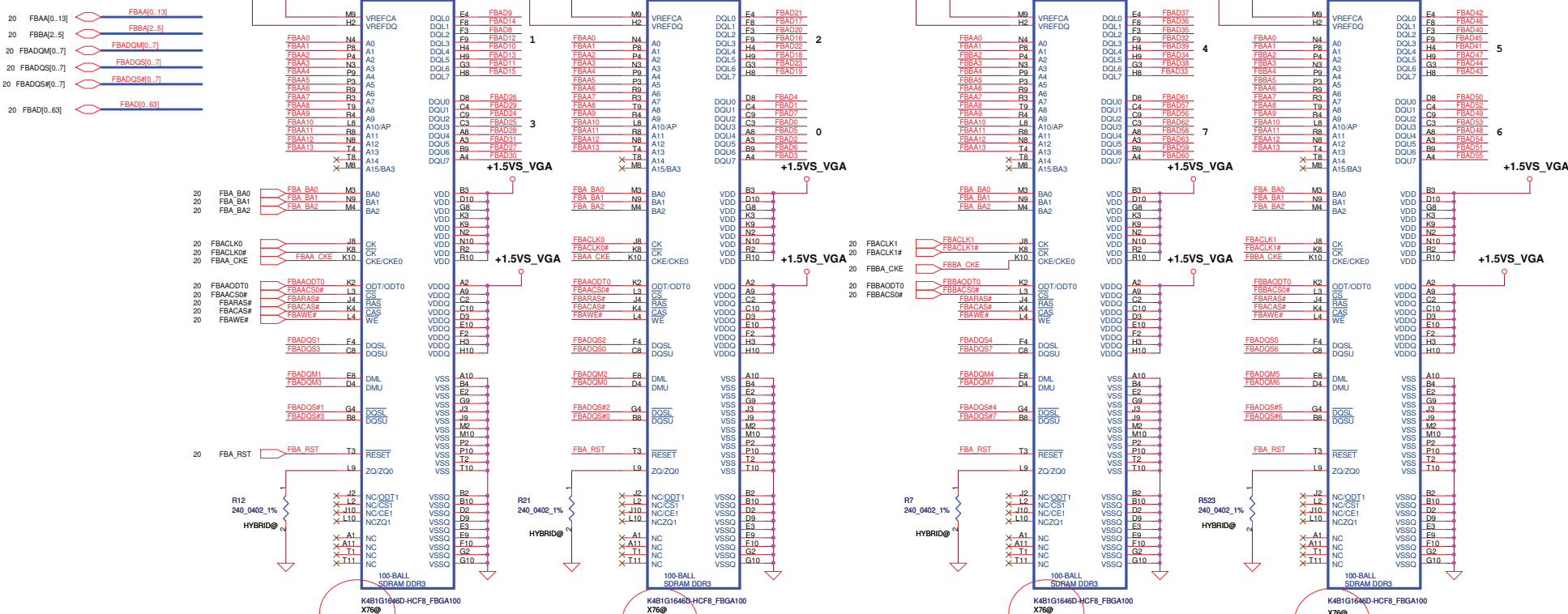
GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
					X76			



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				Date: Thursday, April 08, 2010		
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**N10x 40nm DDR3 MAPPING**  
**NVIDIA DOCUMENT FOR DA-3978-001**



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								<b>VRAM DDR3</b>	
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Size C		Document Number						Rev 0.3	
		<b>LA-5941P</b>							
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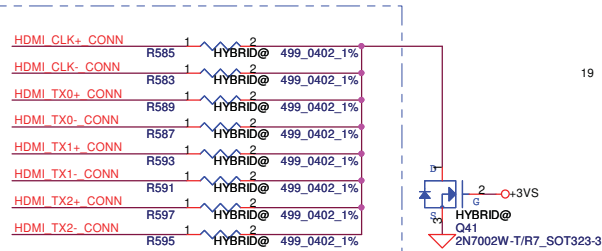
## From VGA

20	VGA_HDMI_CLK+	C284	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_CLK+ CK
20	VGA_HDMI_CLK-	C283	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_CLK- CK
20	VGA_HDMI_TX0+	C282	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX0+ CK
20	VGA_HDMI_TX0-	C281	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX0- CK
20	VGA_HDMI_TX1+	C601	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX1+ CK
20	VGA_HDMI_TX1-	C600	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX1- CK
20	VGA_HDMI_TX2+	C614	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX2+ CK
20	VGA_HDMI_TX2-	C599	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX2- CK

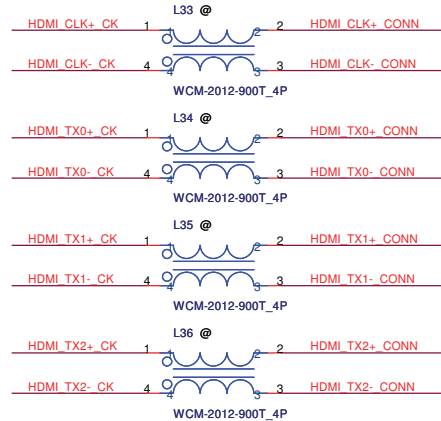
Near L33, L34, L35, L36

## From Level Shiftter

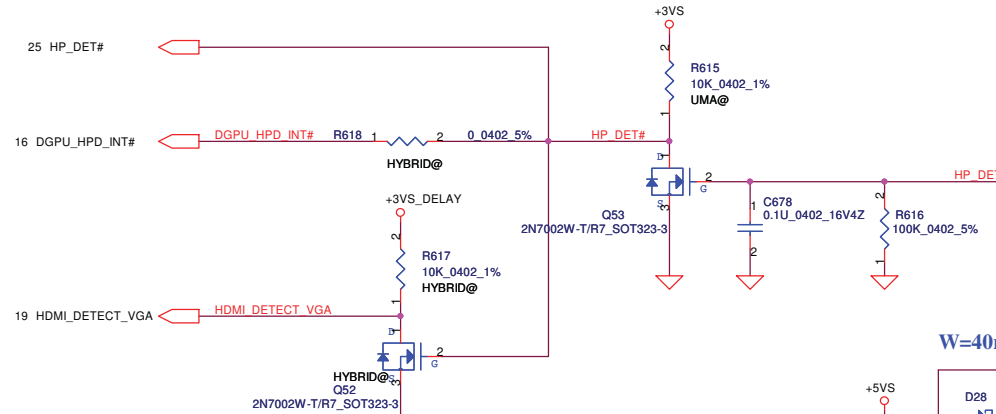
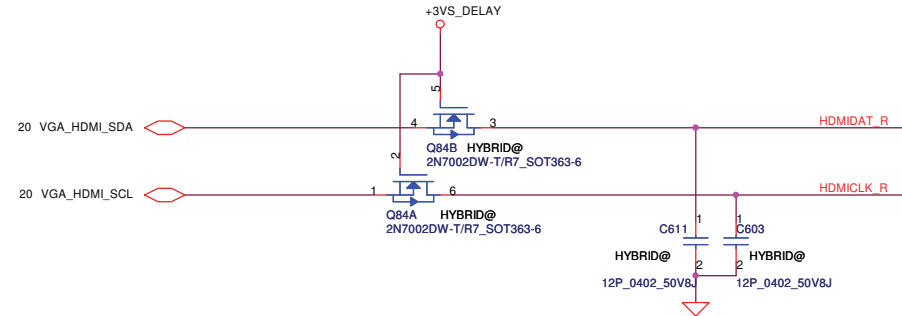
25	HDMI_CLK+ CK	HDMI_CLK+ CK
25	HDMI_CLK- CK	HDMI_CLK- CK
25	HDMI_TX0+ CK	HDMI_TX0+ CK
25	HDMI_TX0- CK	HDMI_TX0- CK
25	HDMI_TX1+ CK	HDMI_TX1+ CK
25	HDMI_TX1- CK	HDMI_TX1- CK
25	HDMI_TX2+ CK	HDMI_TX2+ CK
25	HDMI_TX2- CK	HDMI_TX2- CK



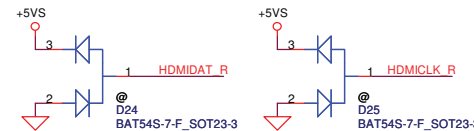
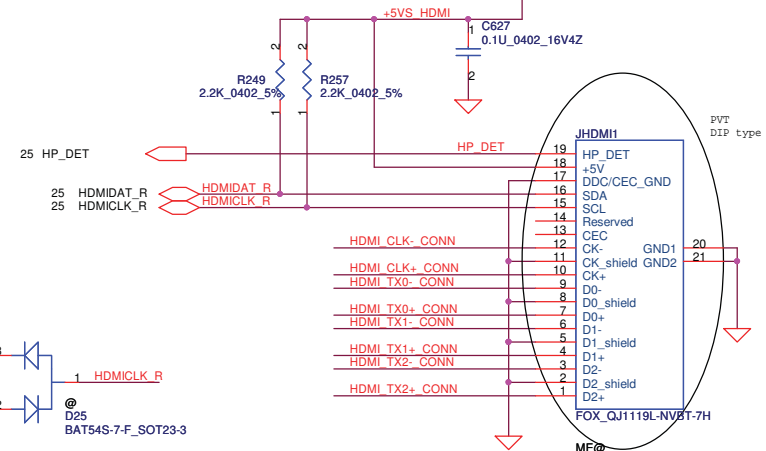
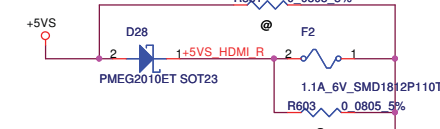
## NEAR CONNECT



HDMI_CLK+ CK	R584	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_CLK- CK	R582	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI_TX0+ CK	R588	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_TX0- CK	R586	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI_TX1+ CK	R592	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_TX1- CK	R590	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI_TX2+ CK	R596	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_TX2- CK	R594	1	2	0.0402_5%	HDMI_TX2- CONN

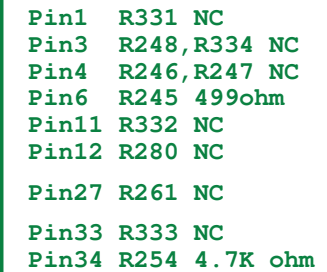


W=40mils



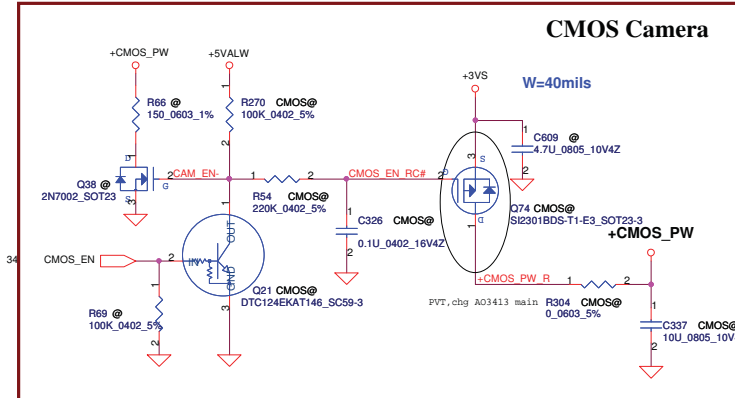
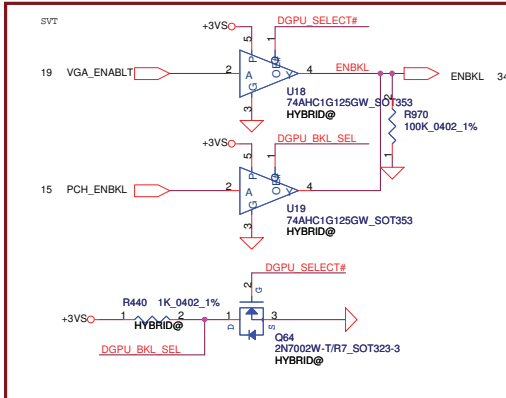
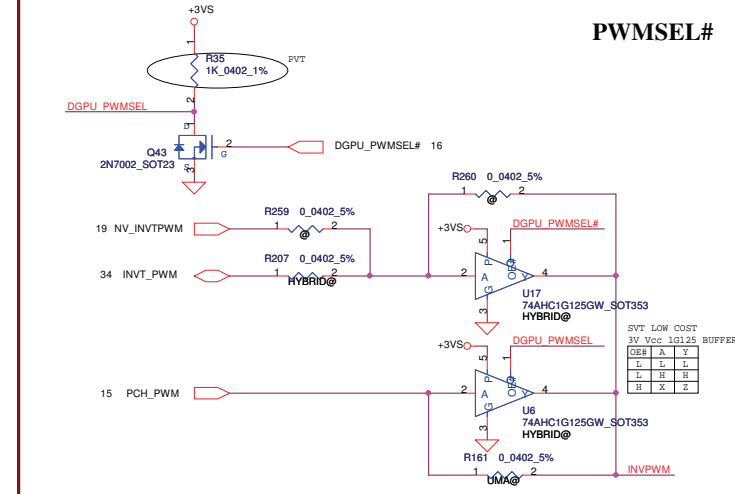
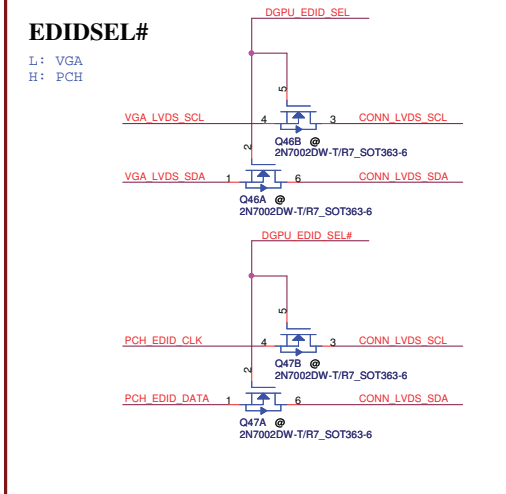
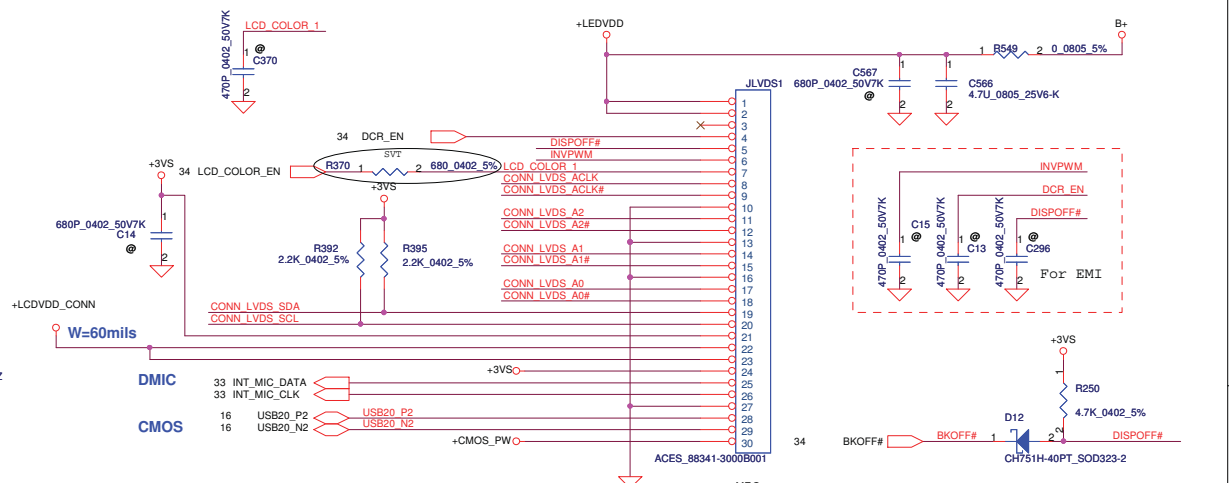
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RESERVE THE R668 PULL UP TO 3VS  
RESERVE THE R670 PULL DOWN TO GND  
CHANGE R245 FROM 499 TO 3.4K OHM



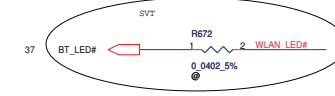
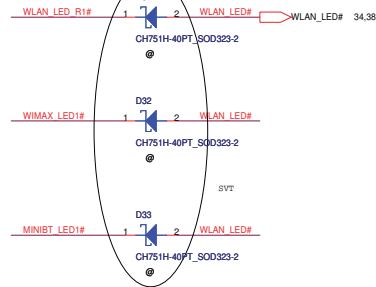
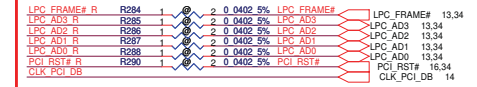
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				Level Shifter _ASM1442		
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### Mini-Express Card(WLAN/WiMAX)



**Mini-Express Card (WWAN 3G)**

The diagram illustrates the electrical connections for the Mini-Express Card (WWAN 3G). The card is identified as H=4.0mm, P/N: DC020910200.

**Power Supply Connections:**

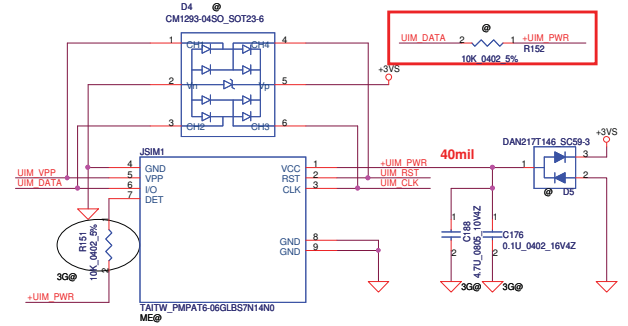
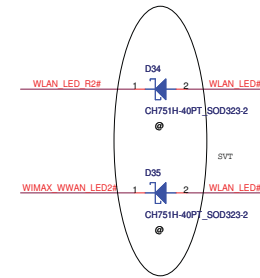
- +3VS:** Connected to pin 2 of JPCIE2 and pin 1 of R368.
- +1.5VS:** Connected to pin 1 of R88.
- +3VSW:** Connected to pin 2 of R367 and R369.

**Signal Connections:**

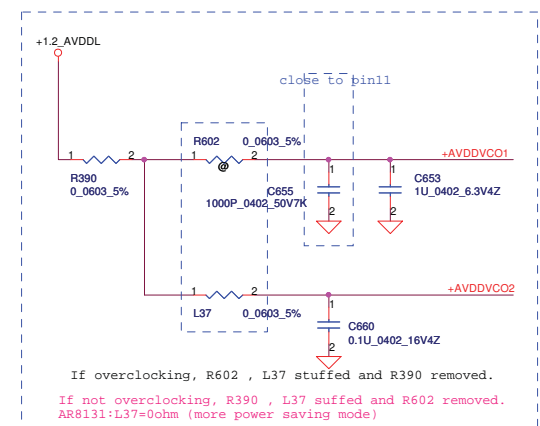
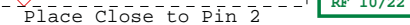
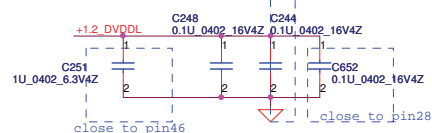
- PCIe:** JPCIE2 connector pins 1-16 are connected to the card's JPCIE2 pins 1-16. The card's JPCIE2 pins 17-54 are connected to the card's internal components.
- USB:** USB20\_N13 and USB20\_P13 are connected to the card's USB20\_N13 and USB20\_P13 pins.
- WWAN:** WWAN\_WWAN\_LED2# and WWAN\_LED\_RSG are connected to the card's WWAN\_WWAN\_LED2# and WWAN\_LED\_RSG pins.

**Other Components:**

- R368:** 3GΩ, 0.0402 5% resistor.
- R367:** 0.0402 5% resistor.
- R369:** 0.0402 5% resistor.
- R366:** 0.0402 5% resistor.
- R365:** 0.0402 5% resistor.
- R417:** 0.1U, 0402, 16V4Z capacitor.
- C419:** 0.1U, 0402, 16V4Z capacitor.
- C418:** 10U, 0805, 10V4Z capacitor.

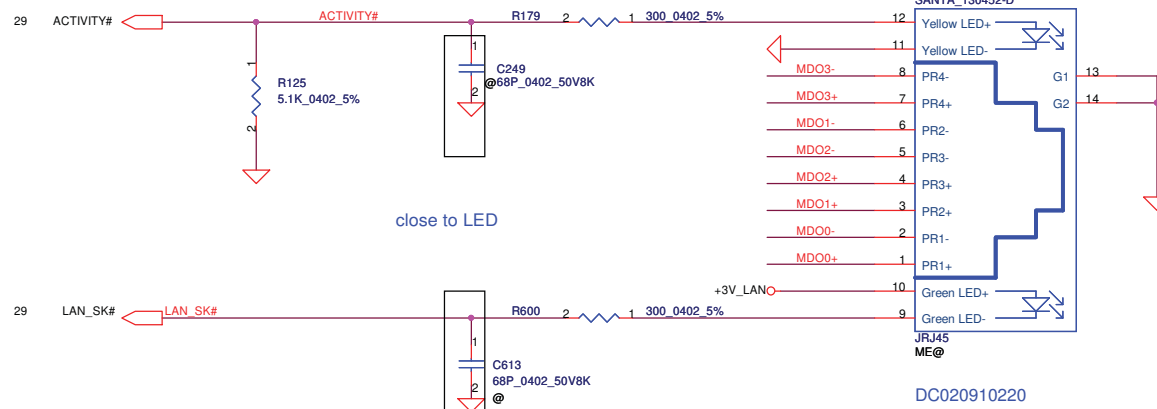
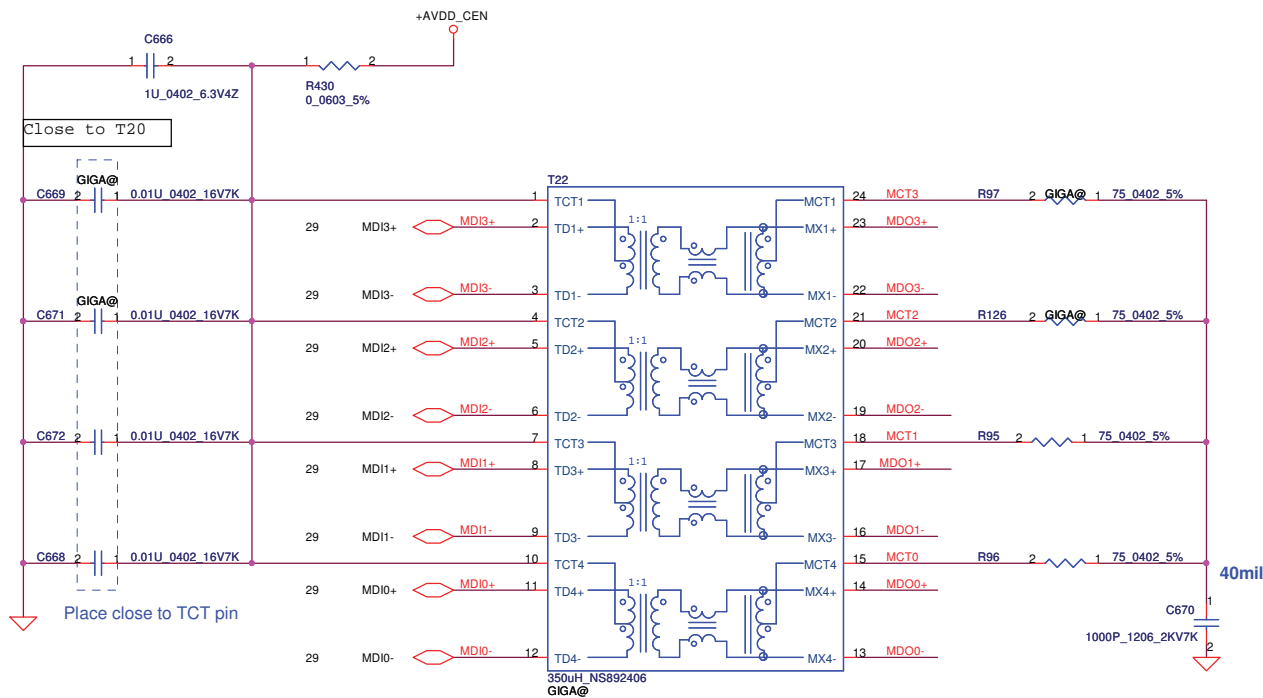
[illegible]

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	45 DA/DSS DA/DSS (NEW)
31	-A (port 1)
32	47 SSD_DET# SSD_DET# (NEW)
33	+A (port 1)



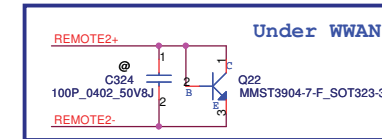
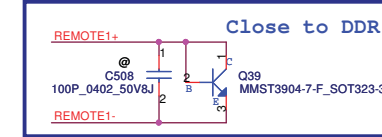
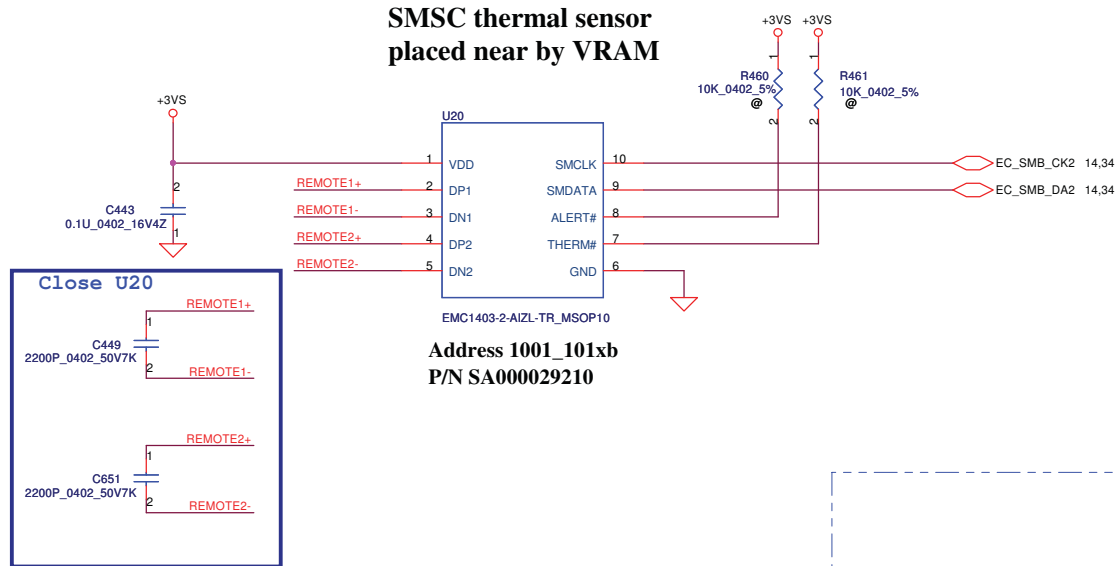
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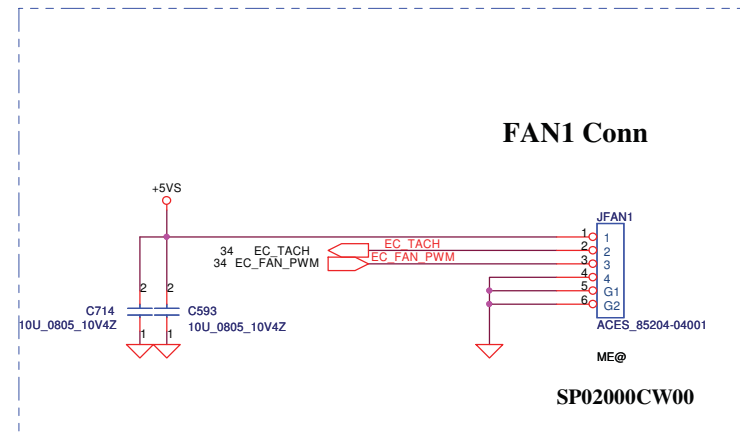


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# SMSC thermal sensor placed near by VRAM

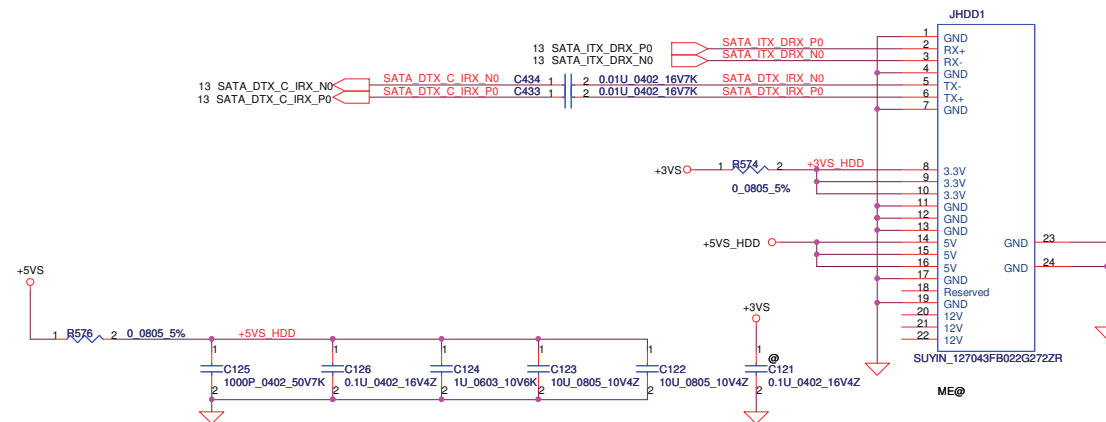


REMOTE1, 2+/-:  
Trace width/space: 10/10 mil  
Trace length: <8"

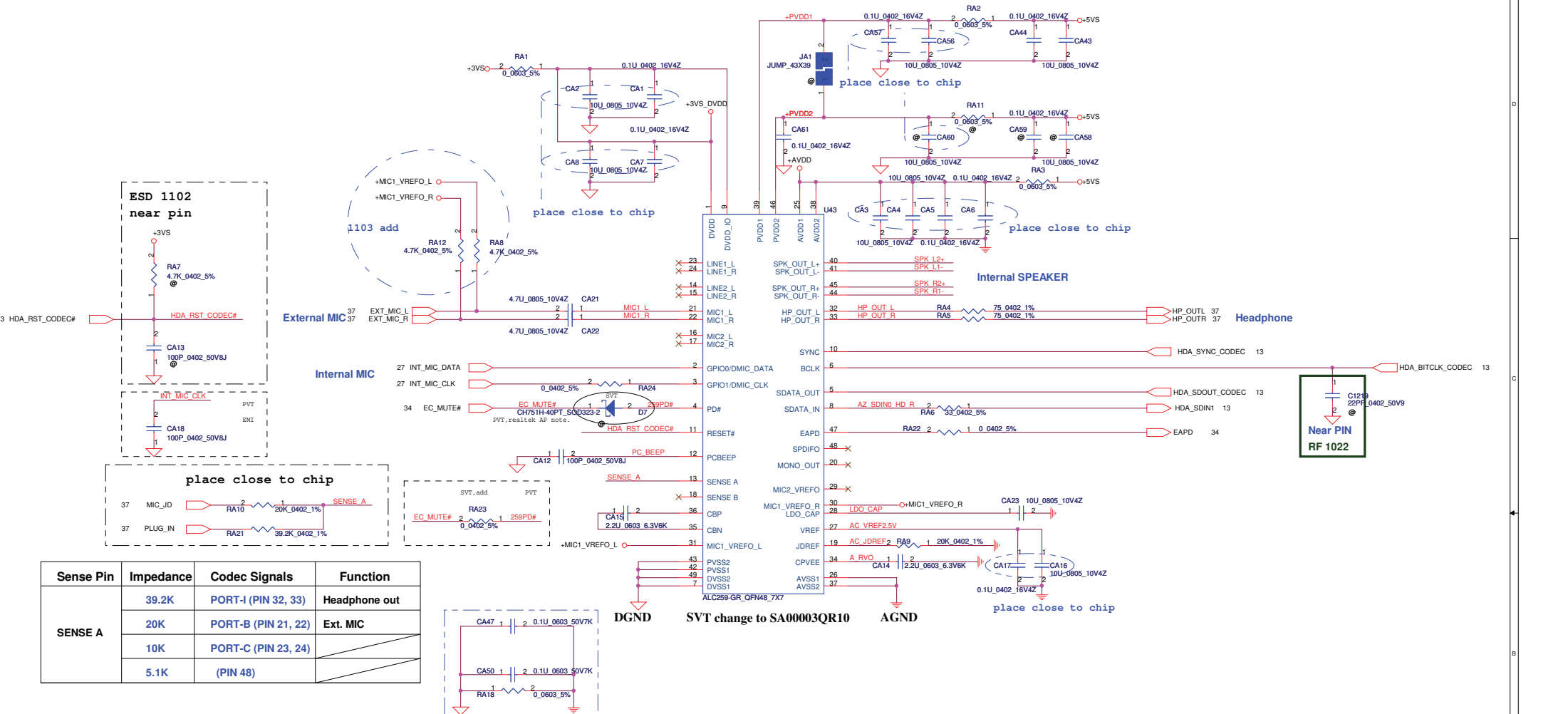


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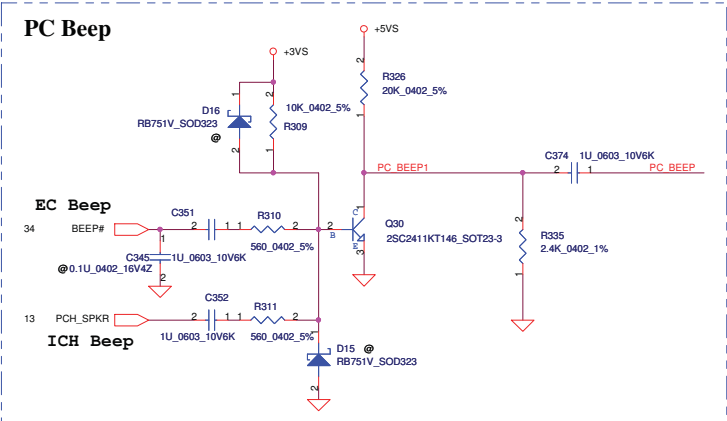
# SATA HDD Conn.



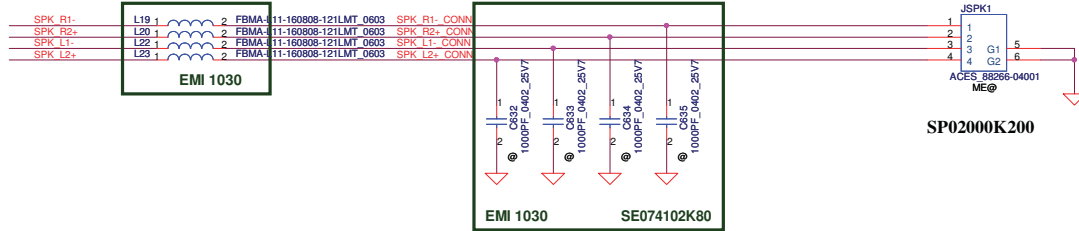
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	HDD/ODD Connector	
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	



wide 20MIL

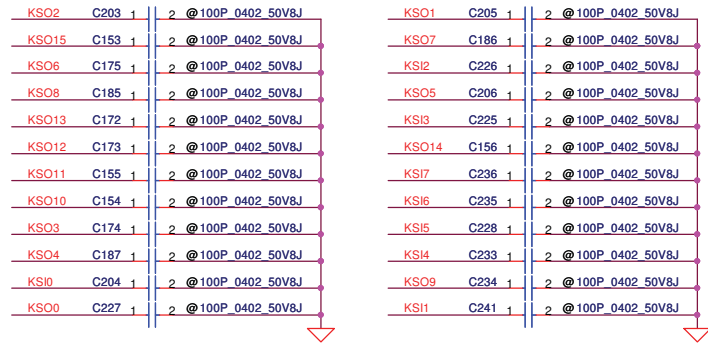


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Date: Thursday, April 08, 2010				Rev 0.3	33 of 50

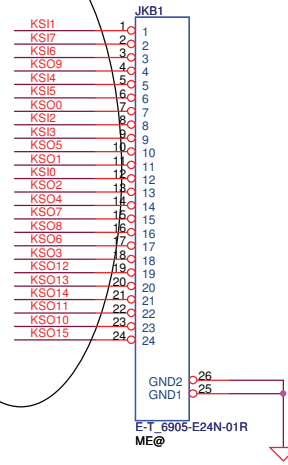


## INT\_KBD Conn.

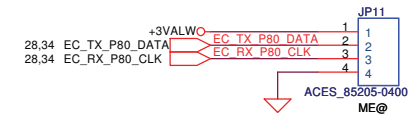
KS[0..7] 34  
KSO[0..15] 34



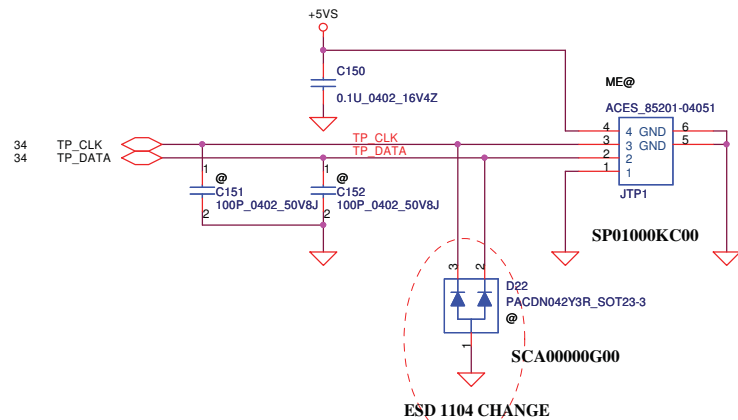
## KB Matrix 10/30



## EC DEBUG PORT



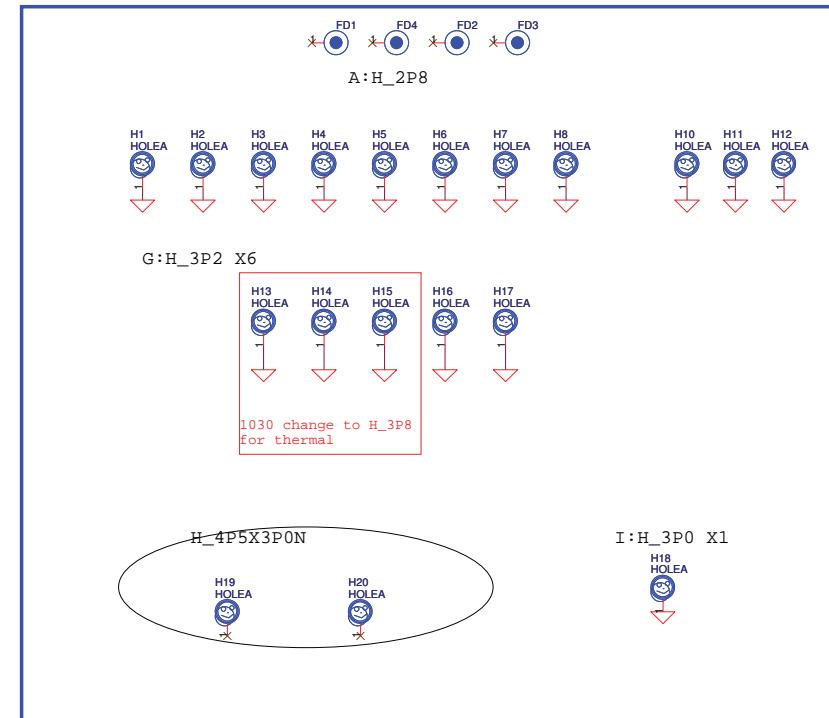
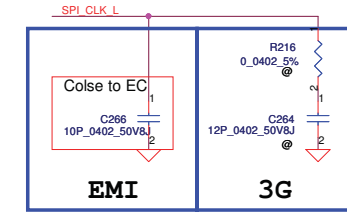
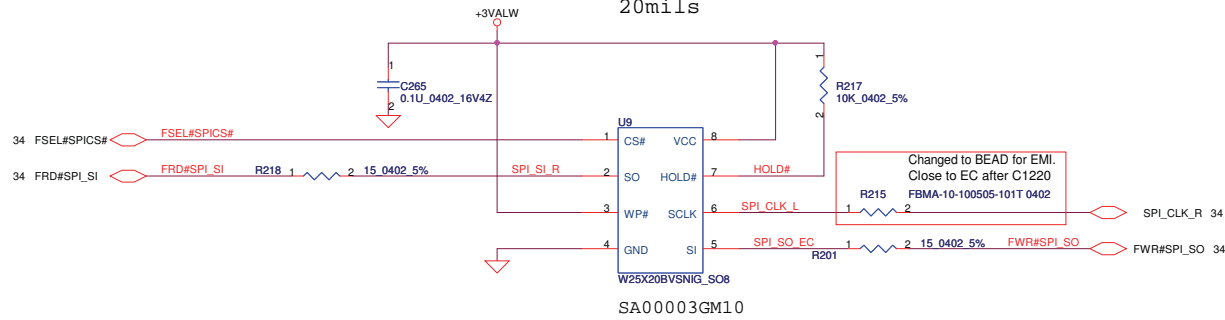
## To TP/B Conn.



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# FOR EC 256KB SPI ROM (150mil PACKAGE)

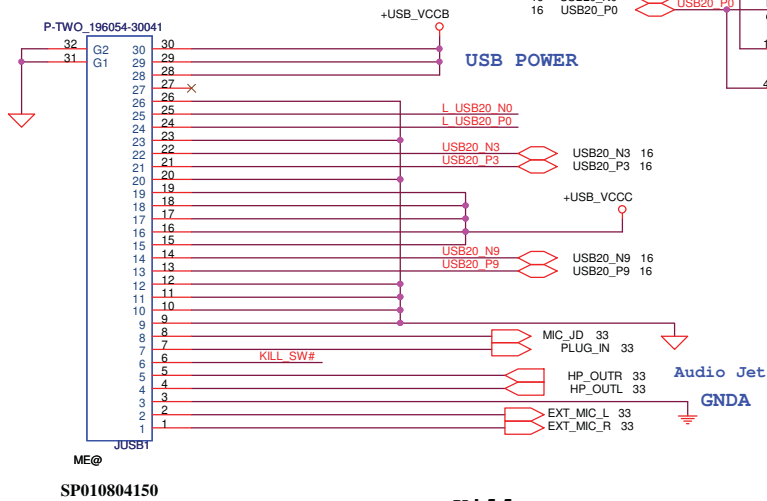
20mils



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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	EC SPI ROM
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				Date:	Thursday, April 08, 2010
				Sheet	36 of 50
				Rev	0.3
				LA-5941P	



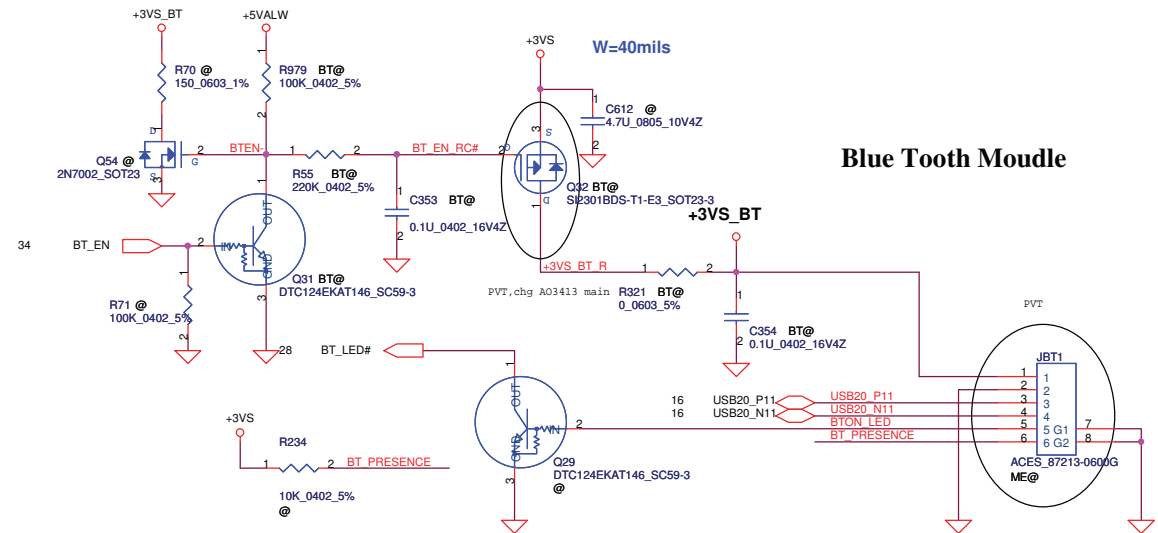
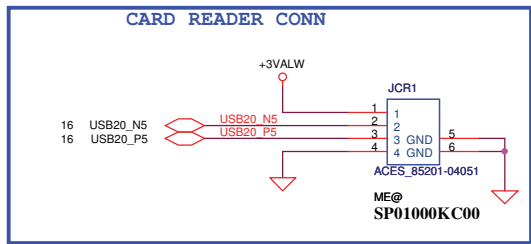
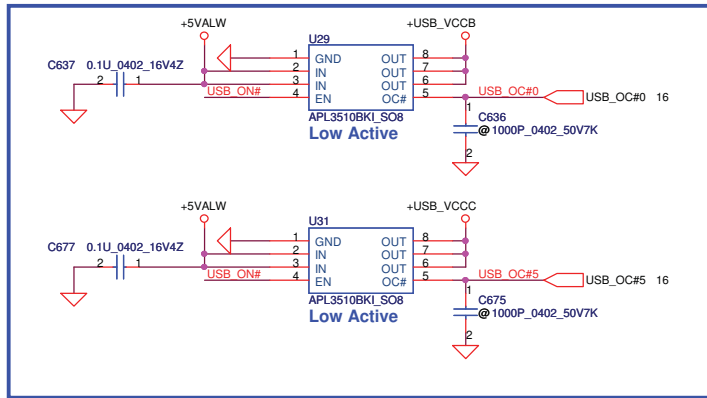
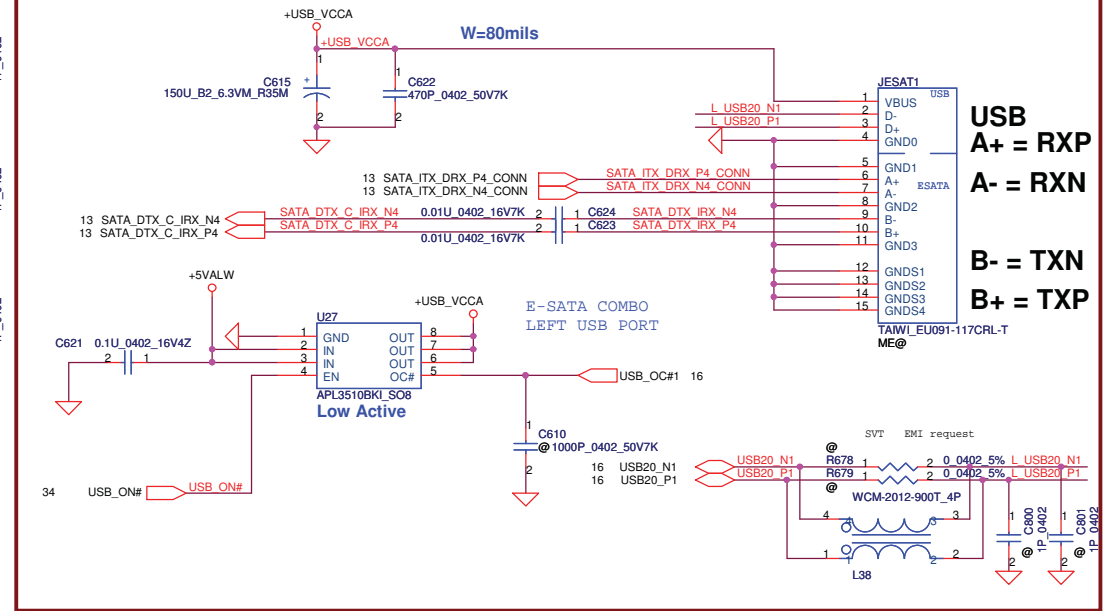
## TO USB BOARD/Audio Jet CONN



### Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

## ESATA and USB Conn.



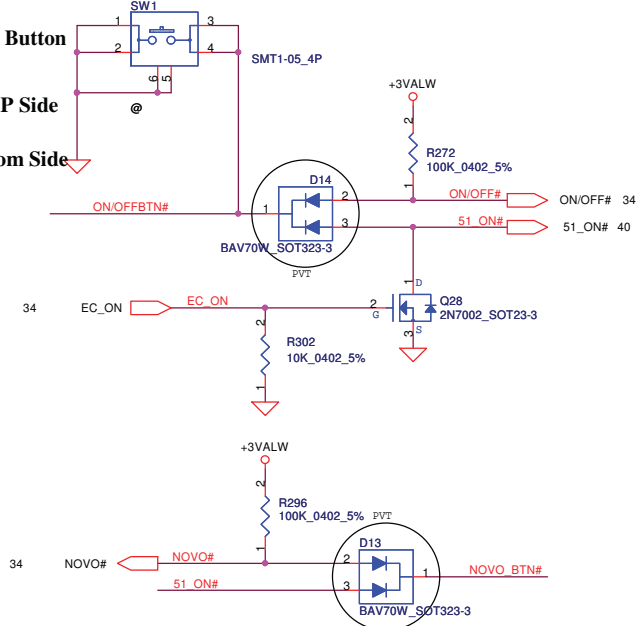
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/01/13				Title			
Deciphered Date				2011/01/13				USB ports/BT/E-SATA			
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				Customer				LA-5941P			
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				50							

## ON/OFF switch FOR DEBUG

Power Button

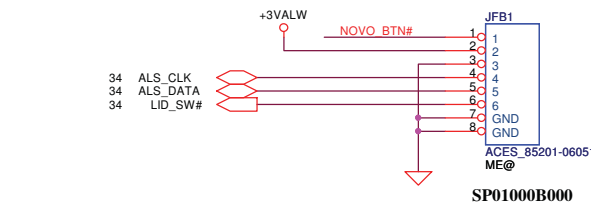
TOP Side

Bottom Side



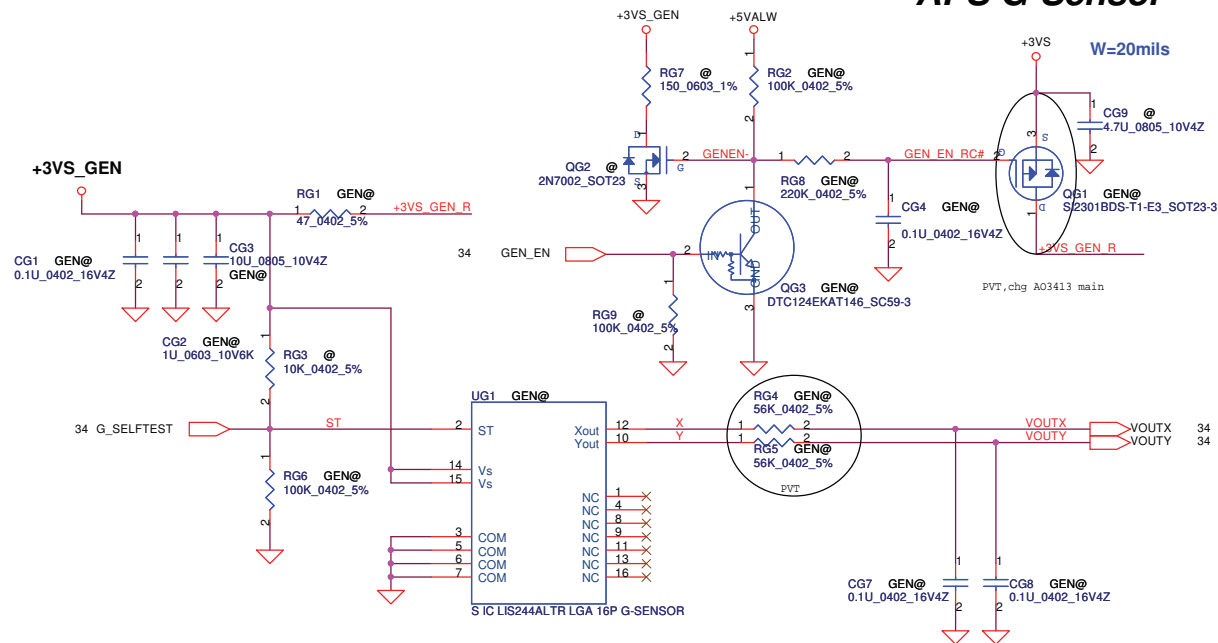
## Power Bottom Board Conn.4pin

## NOVOBottom/ALS Board Conn.6pin

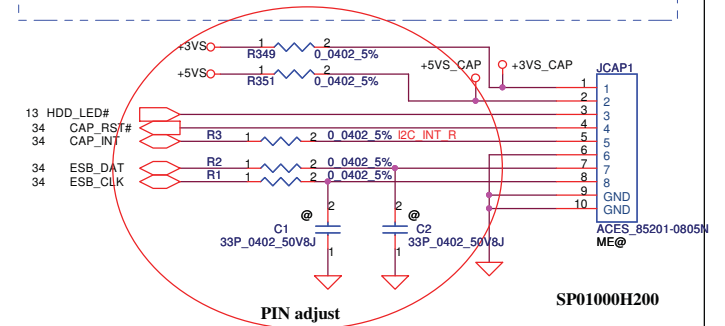


EMI REQUEST 1ST = SCA00000E00  
2ST = SCA00000R00

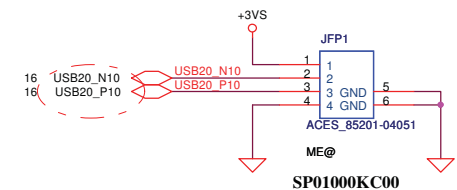
## APS G-Sensor



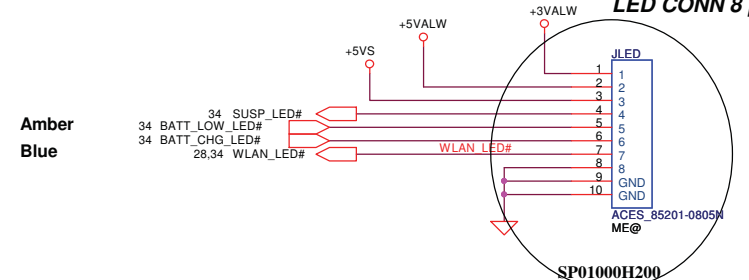
## Cap Sensor Board Conn. 8pin ENE SB3534



## FP Board Conn 4 pin



## LED CONN 8 pin



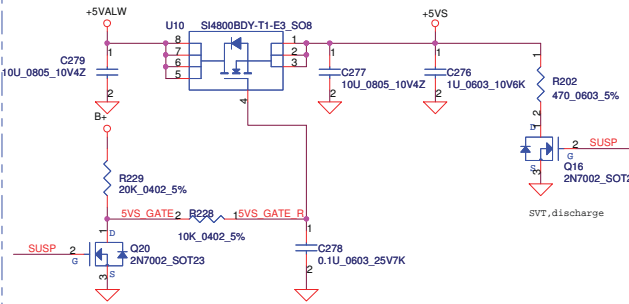
Amber  
Blue



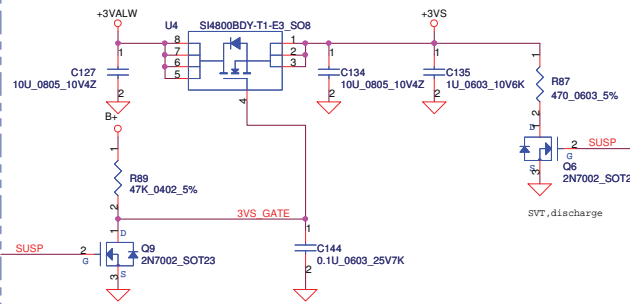
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	Audio Jack & SW connector
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				LA-5941P	
				Date: Thursday, April 08, 2010	Sheet 38 of 50

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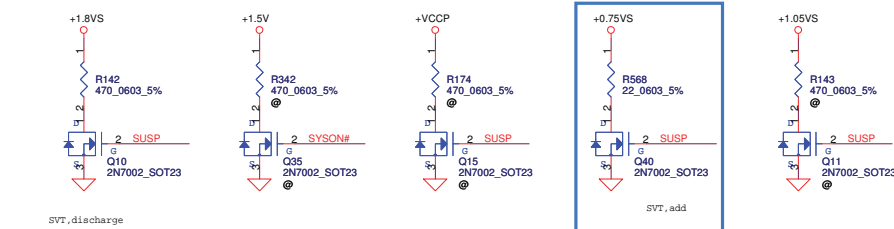
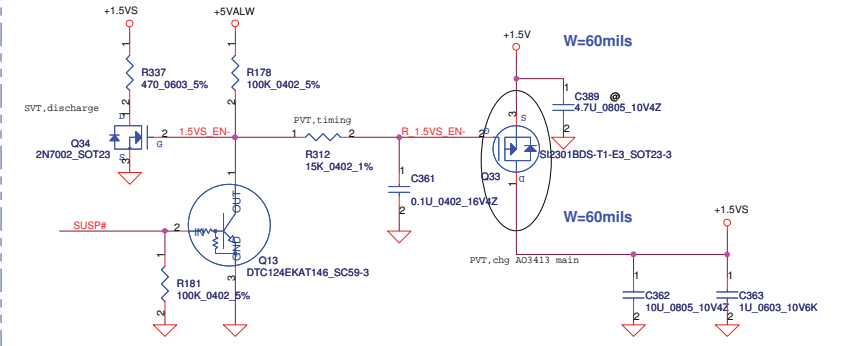
# +5VALW TO +5VS



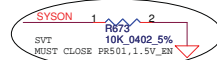
# +3VALW TO +3VS



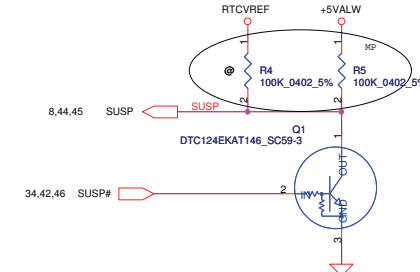
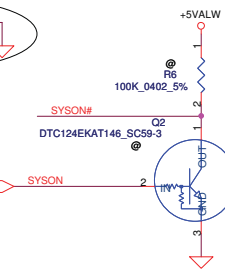
# +1.5V to +1.5VS



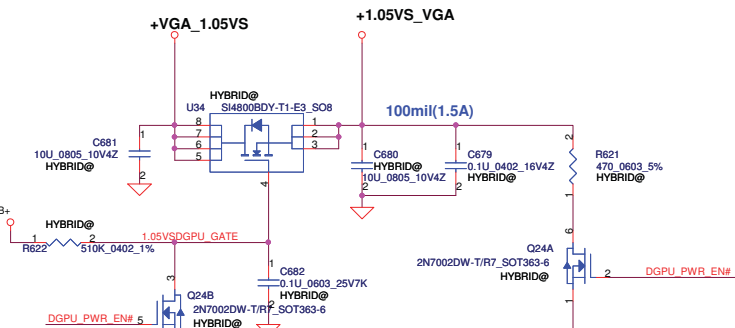
For Intel S3 Power Reduction.



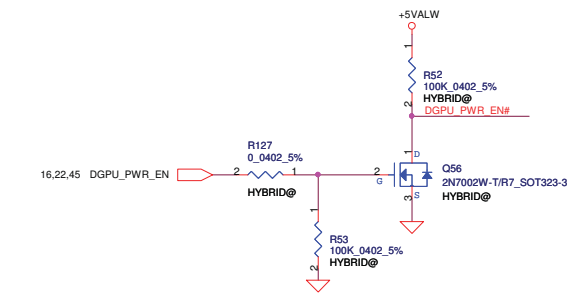
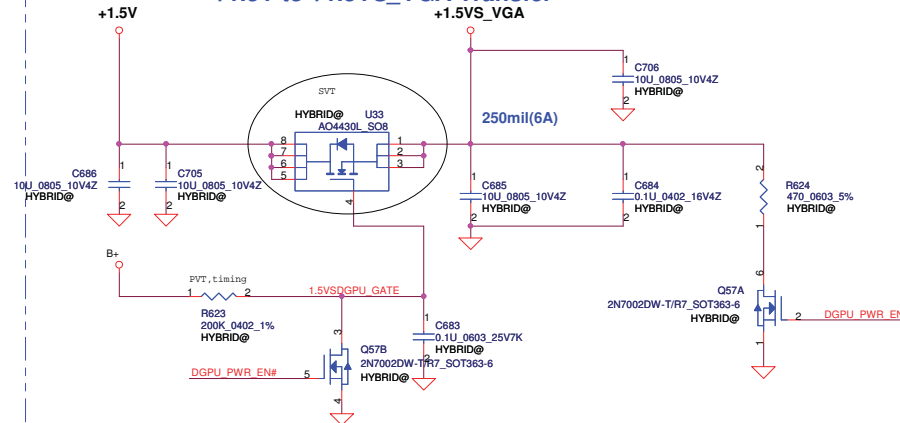
34.44



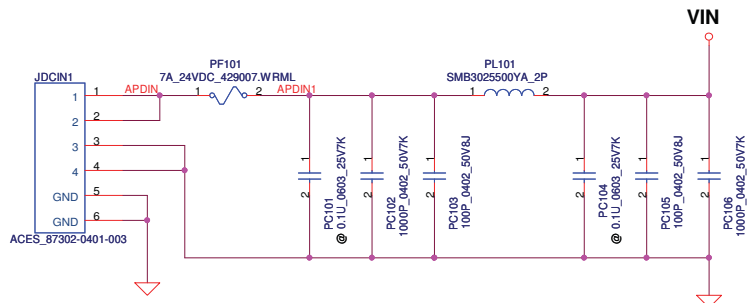
# +1.05VS to +1.05VS\_VGA Transfer



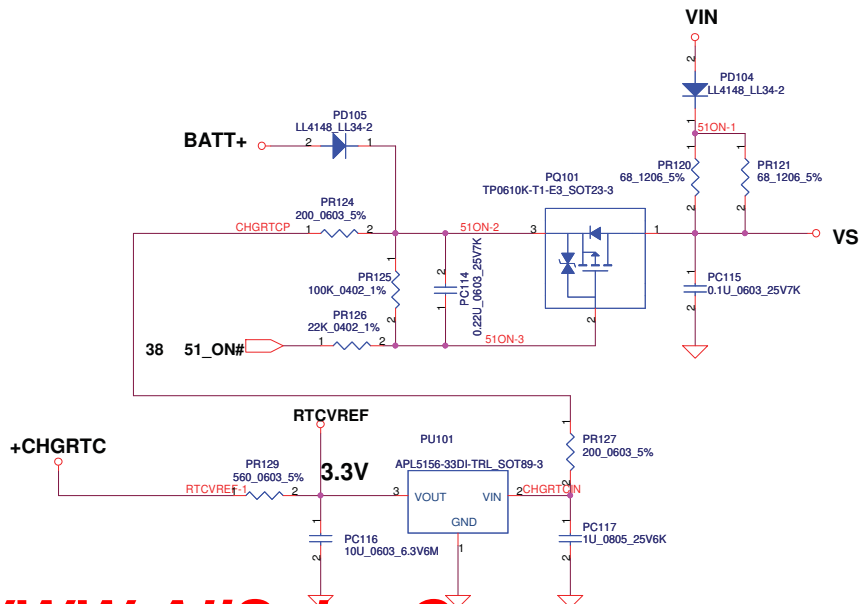
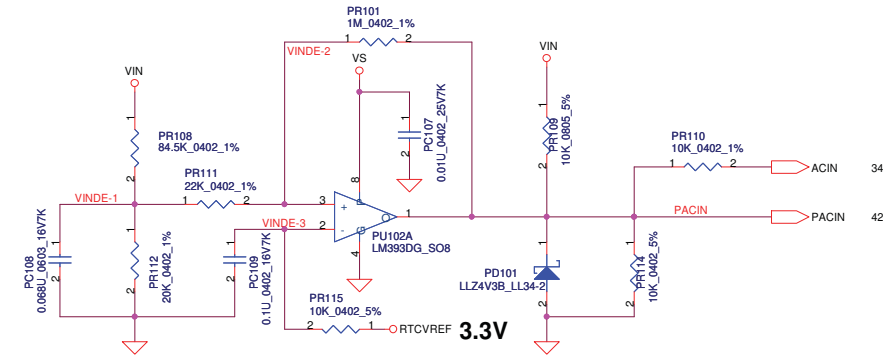
# +1.5V to +1.5VS\_VGA Transfer



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Issued Date		Deciphered Date		Title	
2010/01/13		2011/01/13		DC Interface	
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		Custom		0.3	
		Date:		Thursday, April 08, 2010	
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	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

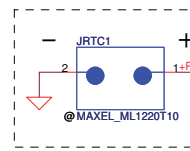
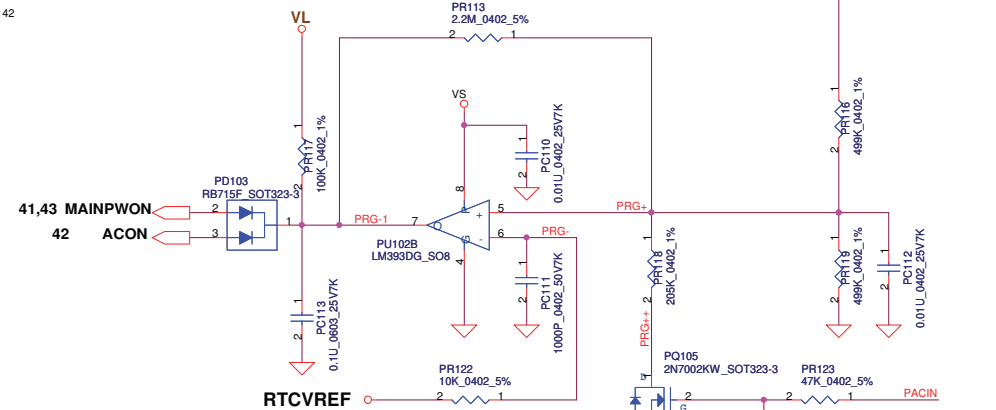
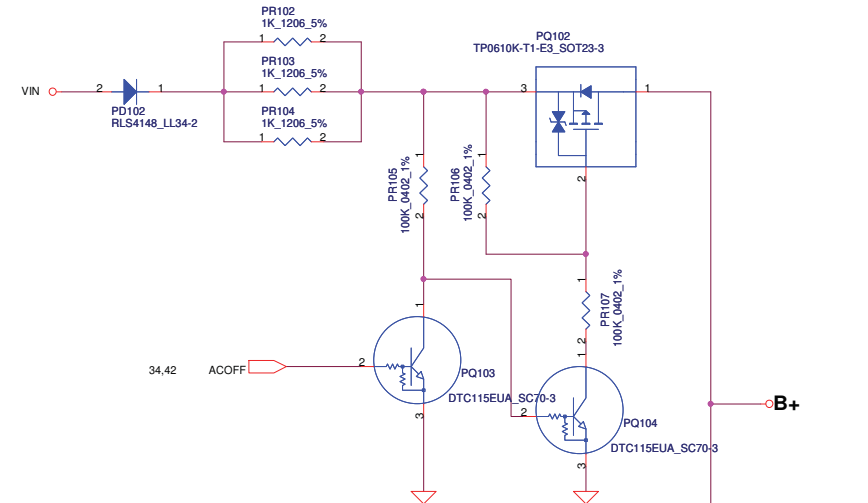


## ACIN

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

## BATT ONLY

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

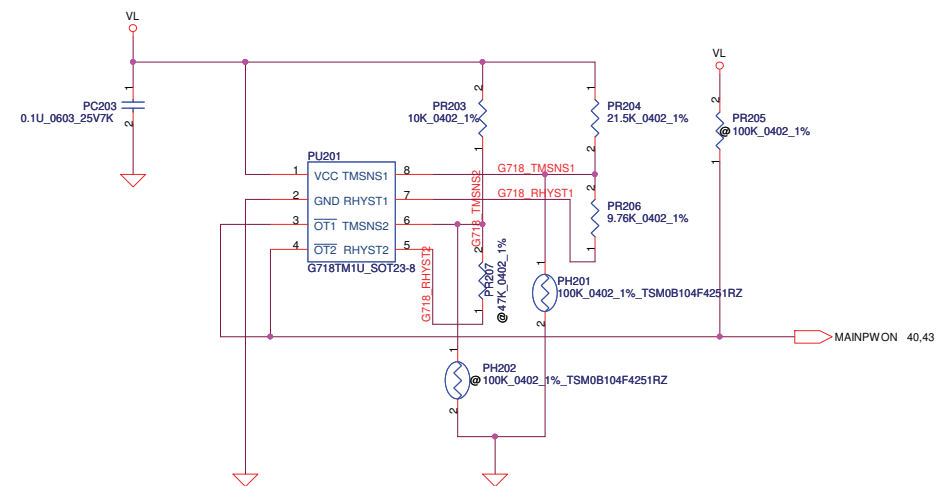
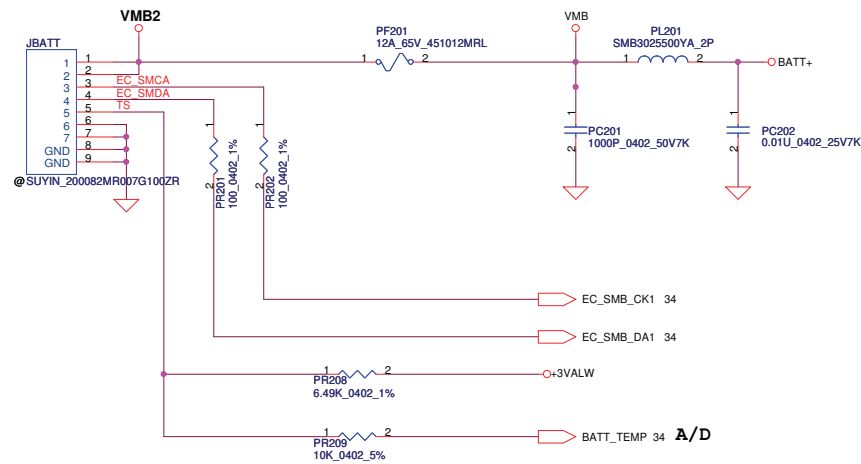


RTC Battery

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/01/13				Title			
Deciphered Date				2011/01/13				DCIN & DETECTOR			
Size				Document Number				Rev			
Custom								0.3			
Date:				Thursday, April 08, 2010				Sheet			
				40				of			
				50							

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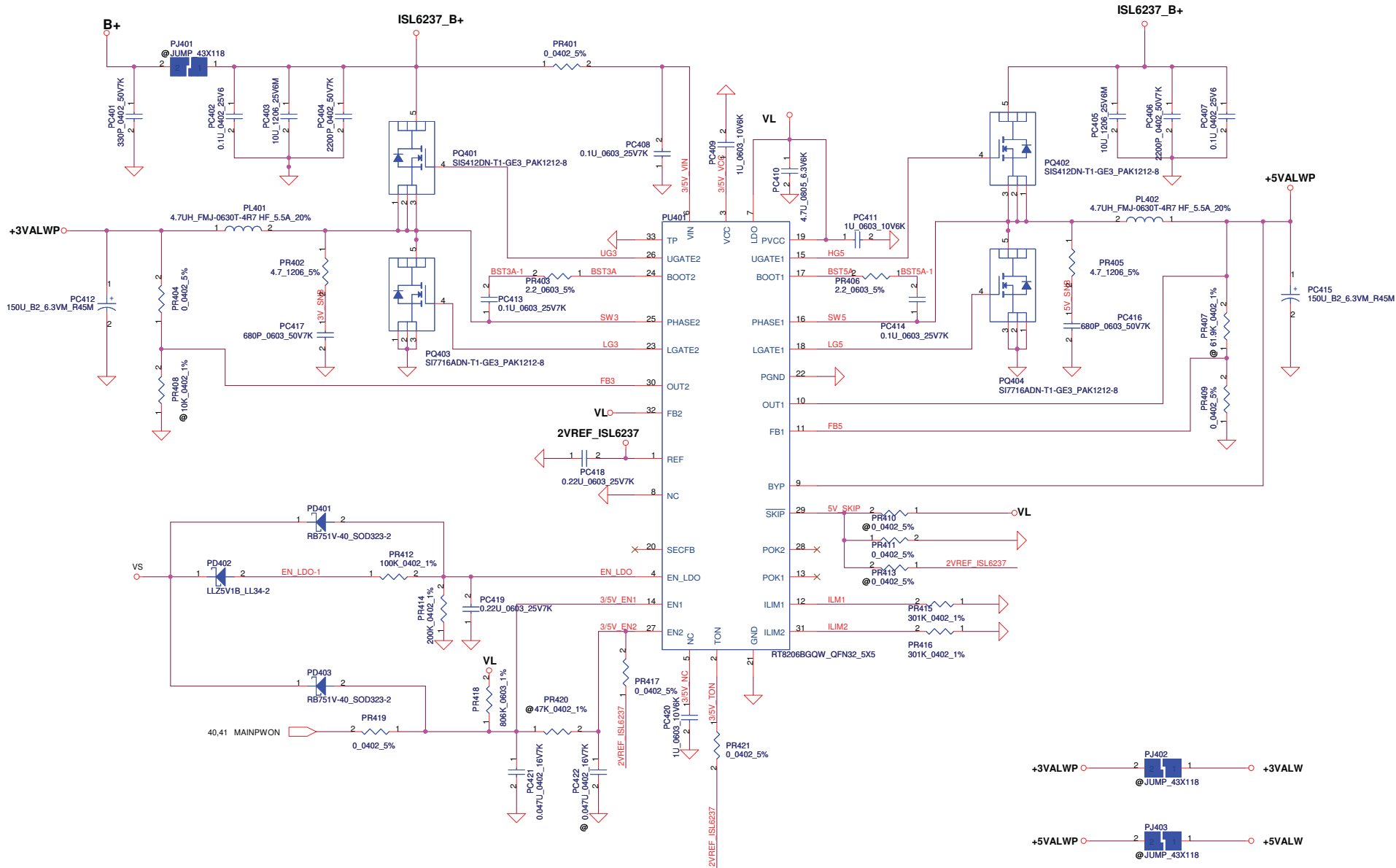
PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C

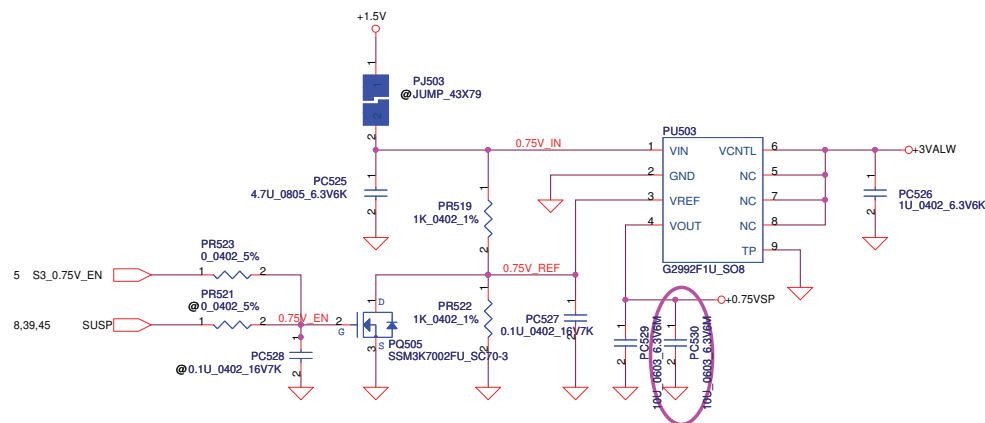
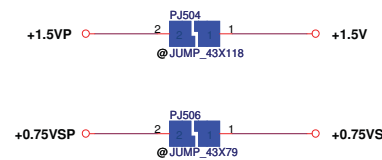
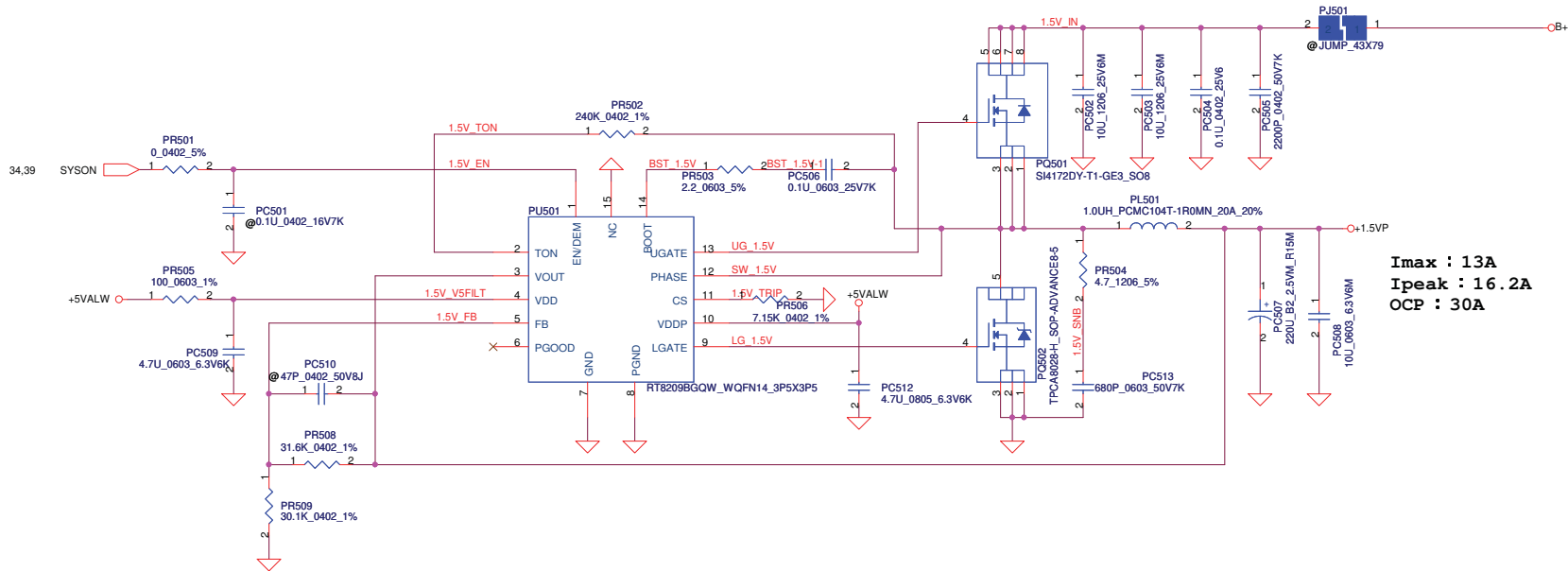


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Size		Document Number			Rev
Date:		Thursday, April 08, 2010			0.3
Sheet		41 of 50			

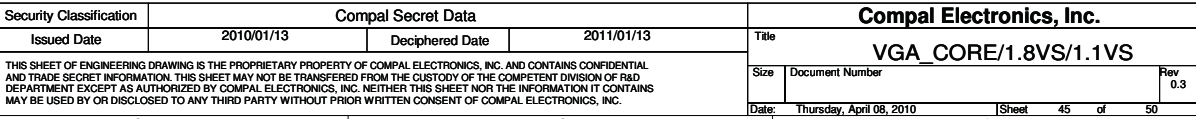


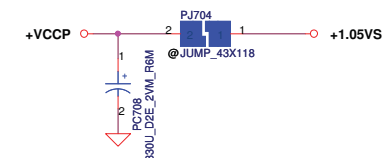
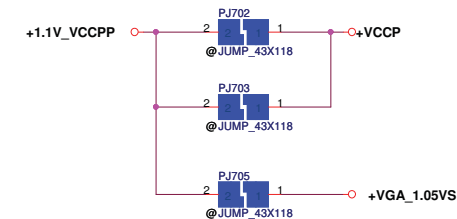
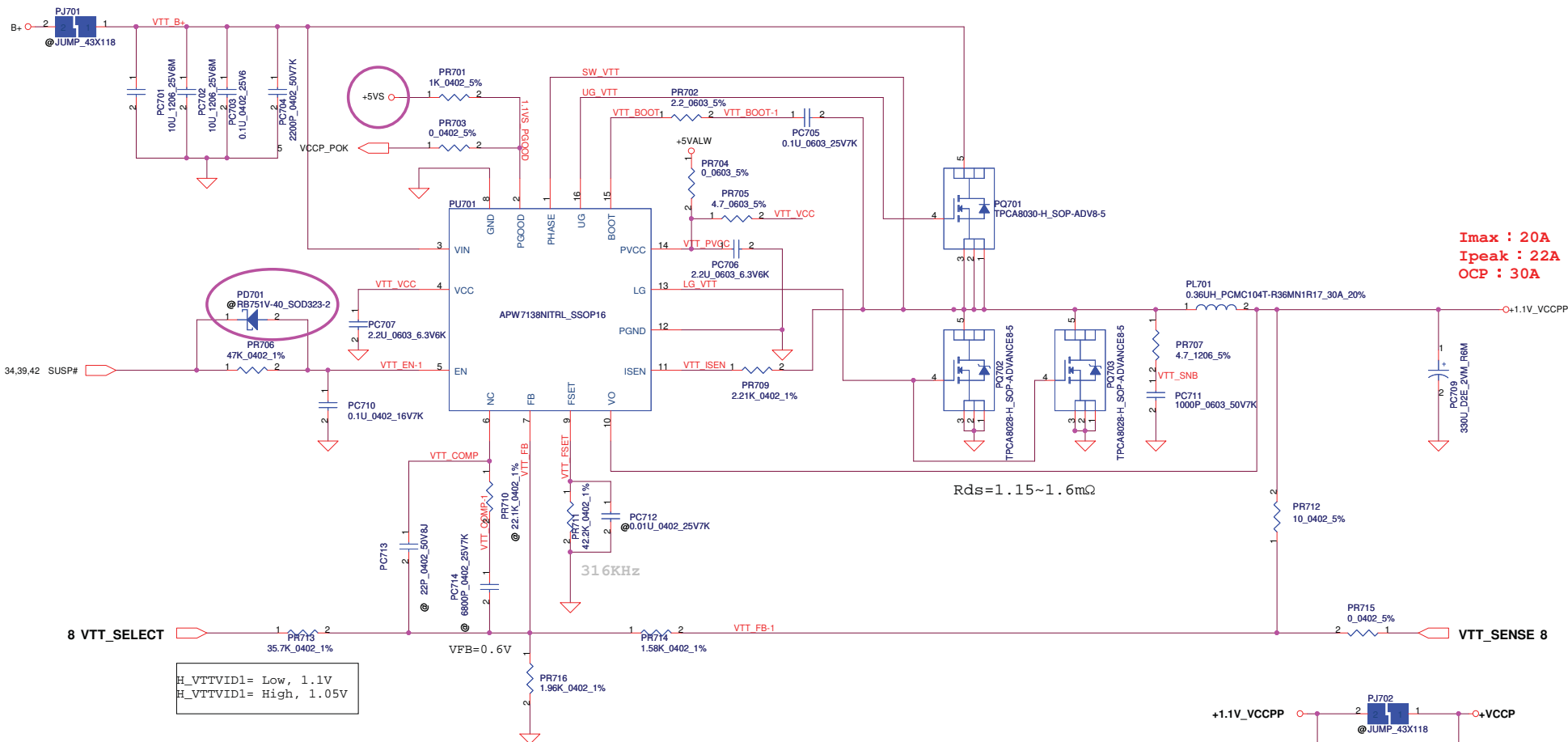






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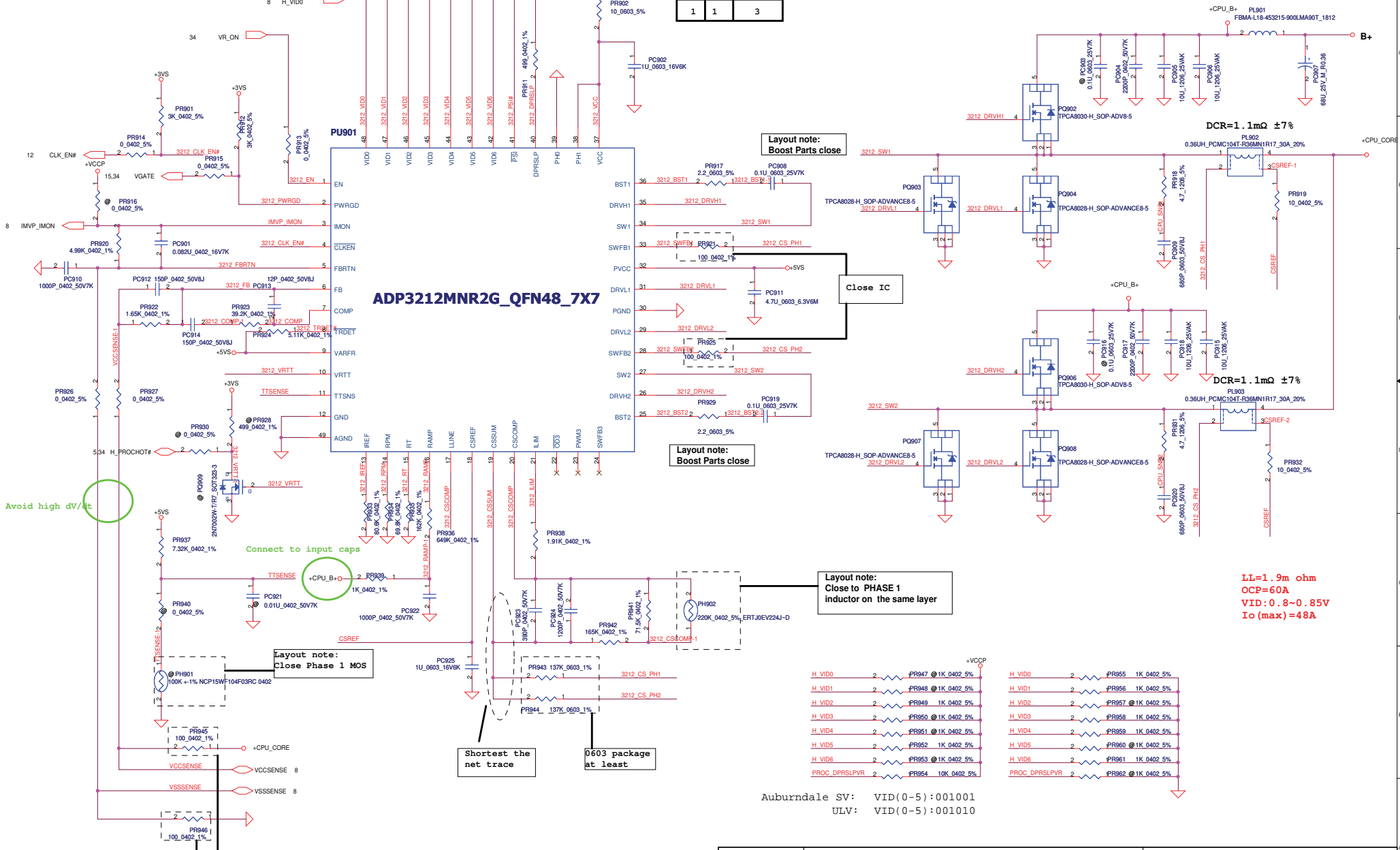
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	
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Custom					
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8 PROC\_DPRSLPVR  
8 PSIF  
8 H\_VID6  
8 H\_VID5  
8 H\_VID4  
8 H\_VID3  
8 H\_VID2  
8 H\_VID1  
8 H\_VID0

PH0	PH1	# of PH
0	0	1
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	0.85	50	1.9m	37	35
Auburndale 35W	0.85	38	1.9m	29	27
Clarksfield SV	0.95	52	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Auburndale SV: VID(0-5):001001  
ULV: VID(0-5):001010

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add S3_0.75V_EN for 0.75 enable singal	44	Add PR523 and reserve PR521	11/09	Before A
2	Modify VGA GPIO table for NVIDIA SPEC.	45	Reserve PR615, PR617, PR618 and PC617 PR612, PR613 change to 84.5K from 100K	11/09	Before A
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	



5				4				3				2				1				
NO DATE		PAGE		MODIFICATION LIST				PURPOSE		NO DATE		PAGE		MODIFICATION LIST				PURPOSE		
-----																				
1	30	RJ45 CONNECTOR				VER. R0_1030			1	PVT	24	HDMI connector change to DIP type				DFB request				
2	35	KB Matrix change							2	PVT	28	R336 change to 100Kohm				BOM error				
3	31	EMC1403-1 change to EMC1403-2							3	PVT	38	D13,D14 change to panjit				cost down				
4	40, 42	POWER modify PQ313, PU102							4	PVT	38	RG4,RG5 chagne 56k ohm				RC filter for G-sensor output, EC request.				
5		change USB port				FP : port10			5	PVT	37	JBT1 change to 6 pin				For 6 pin BT module				
6		change USB power				USB3 : port 9			6	PVT	34	SUSCLK connect to clock out				EC issued change note.				
7									7	PVT	34	R978 45 to 0 ohm				For ECROM can't flash				
1102D MODIFY																				
8	33	Add RA7, CA13				FOR ESD			10	PVT	34	32.768KHz change to 70x15x1.4				cost down				
9	35	Add D22							11	PVT	13	32.768KHz change to 70x15x1.4				cost down				
10	38	JFIR CONN. CHANGE TO 12 PIN							12	PVT	33	INT_MIC_CLK add CA18 100pF cap.				EMI request				
11	36	CHANGE NET NAME							13	PVT	33	Audio pin4 add D7				Realtek change note for bug				
12	27	JLVDS1 CONN. PIN SWAP.							14	PVT	28	Add Q45 2N7002				For Wimax LED no function, bug				
13	13	DEL CLRP1							15	PVT	27	change U42 to ST				cost down				
1104DMODIFY																				
14	16	Add U15, R173, R177, R178, R627, R628							16	PVT	27	Add Q64,Q37,R440				cost down, enable bkl circuit				
1105DMODIFY																				
15	28	Add Q44, Q45, Q49, Q55, Q60, Q62, R336							17	PVT	26	Add R322,R328 0 ohm				For "non-PnP device" bug				
16	26	Add Q61, Q63							18	PVT	22	Add R474 34.8K ohm				N-vidia N11M-LP1 device ID				
17	29	R726 change to 0805							19	PVT	19	L7,L8,L17,L18 change to 0 ohm				for EDID can't detect sometime, cost down				
18	25	Add R559							20	PVT	17	R208 change to 1 ohm				CRT garbege in uma mode				
19	15	Add R180							21	PVT	16	R580 add 0 ohm				for bug, uma switch to dis will hang up				
20	14	Add T24 PAD, T25 PAD							22	PVT	15	R175 2.2k to 4.7k ohm				common design update				
21	8	Add R282							23	PVT	12	Y1 14.318MHz change to 5032 size				common design				
22	14	Add R327, R325, T21 PAD							24	PVT	09	C75,C76,C92,C164 change to 333uF 6m ohm				cost down				
23									25	PVT	X	Q4, QG1, Q32, Q33, Q73, Q74, Q75, Q97 change to A03413				cost down				
24									26	PVT	34	Add R345 10Kohm				EC_TACH pull up				
1109DMODIFY																				
25	14	Del R81, R83							NO DATE		PAGE		MODIFICATION LIST				PURPOSE			
26	16	Add T26 PAD, C687							-----											
27	27	Add R371, R372							1	SVT	39	Add R568, Q40				+0.75VS discharge				
28	34	Del Q26, R303 T21PAD							2	SVT	39	Add R673 10K				+1.5V EN pin pull down				
		Add R230, Q17							3	SVT	39	Change U33 to Low Rds-on type				VRAM voltage drop				
29	26	Del Q61, Q63 Add Q99A, Q99B							4	SVT	37	Add EMI common chock on USB pl,p0;L38,L39				EMI				
5		Add Q61, R416							5	SVT	34	CLKRUN# pull down, R671 10K				common design				
		JFIR CONN change JLED CONN							6	SVT	34	Reserve R685 for WLAN_LED by EC control				WLAN LED				
34		add TP29, R320, R328, R230							7	SVT	33	ALC259 change to VB				Version change				
									8	SVT	29	del R654 leakage				leakage				
									9	SVT	28	WLAN LED control change to DTL AND gate				For some card design				
									10	SVT	27	Add U6, U17, U18, U19 for BKL and PWM control				signal select switch				
									11	SVT	27	Add R370 680ohm				support No color engine panel				
									12	SVT	27	Add D36				LCEVDD discharge				
									13	SVT	26	Reserve CRT double pi filter				Vidio Filter				
									14	SVT	25	Add R670 2.2K				HDMI common design				
									15	SVT	15, 25	Add R675, R674 100K				Hybrid mode disable PCH HDMI				
									16	SVT	17	C505,C492 change size 0603				ME demend				
									17	SVT	17	C447 change to 1uF				common design				
									18	SVT	13	Add R677				HDA SDIN1				
									19	SVT	8	Change R268 to 47K				timing				
									20	SVT	8	Add R551 1K				PSI# pull down, strip pin				
									21	SVT	5	C338 change to 0.047uF				common design, S3 shutdown				
									22	SVT	5	R135 remove				warm boot issue				
									23	SVT	12	Add C365				10pF for RF				
									24	SVT	14	Add R413,C439 22ohm, 10pF				For RF				
NO DATE PAGE MODIFICATION LIST PURPOSE																				
-----																				
1	MP	15	Add R687,R688				Intel DG													
2	MP	39	Add R5, Del R4				S5 power lost													

Title

Size A3

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HW PIR